A Scalable Controller for Power Sources (SCOPS)

Date: June 16, 2025

Speaker: Marc Cousineau

The work is part of the European project SCOPS involving satellite manufacturer teams as well as scientific partners. **Grant agreement No 101082266**.

Funded by the European Union

Horizon 2020
European Union Funding
for Research & Innovation

SCOPS

SCALABLE CONTROLLER FOR POWER SOURCES

AMICSA

European Commission

ThalesAlenia Space
A Thales / Finmeccanica Company

Coordinator & project manager
Architecture / ASIC Design
Radiation & End-user tests

PATENTED

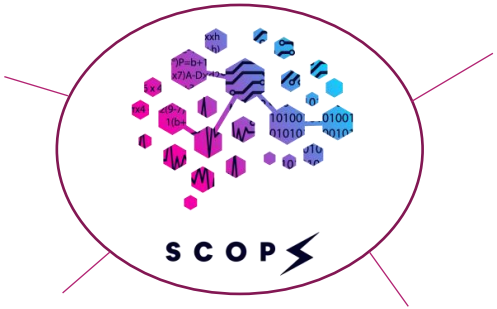
TOULOUSE INP

imec
embracing a better life

DARE180XH library, X-FAB foundry

Laplace

Architecture, Know-how & Patents



ISD Aerospace
Integrated Systems Development

ISD S.A.
Integrated Systems Development

Design & Test validation

Fully Scalable
Microprocessor Power
Supply

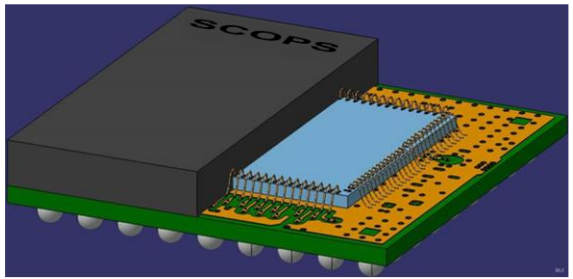
SYNERGIE CAD

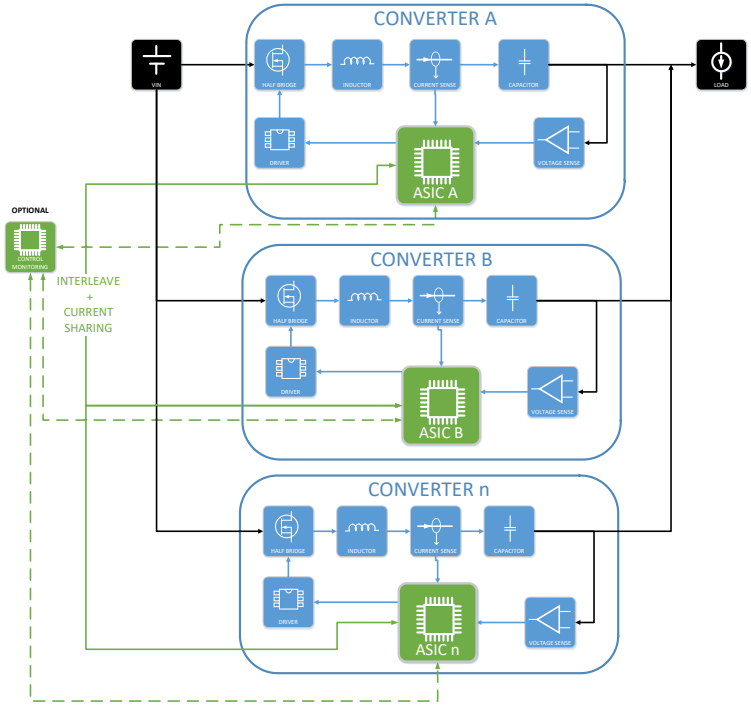
Prototype manufacturing

SCOPS requirements

Main performances goal

- To supply future UDSM ASIC & FPGA (Low voltage High current)
- Power DCDC converter control for low output voltage (≥ 0.6V), high current (≤ 200A)
- Current sharing (parallel operation) up to 10 converters
- 250 kHz to 3 MHz
- Radiation hardened : no SEL, no SEFI, no SET, no SEU and TID 100krad
- Chip size *6mm x 5mm*
- SMD package of BGA 81, 1mm pitch





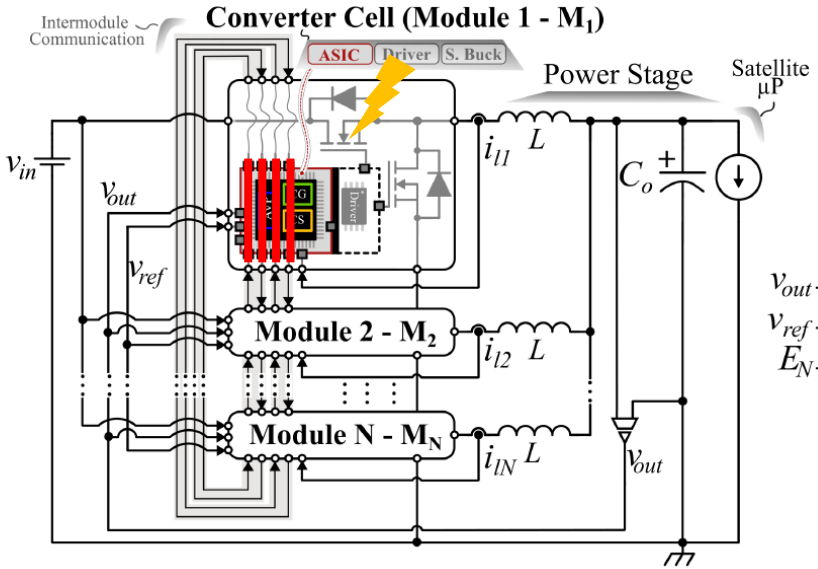
1. INTRODUCTION – DECENTRALIZED CONTROL CONCEPT

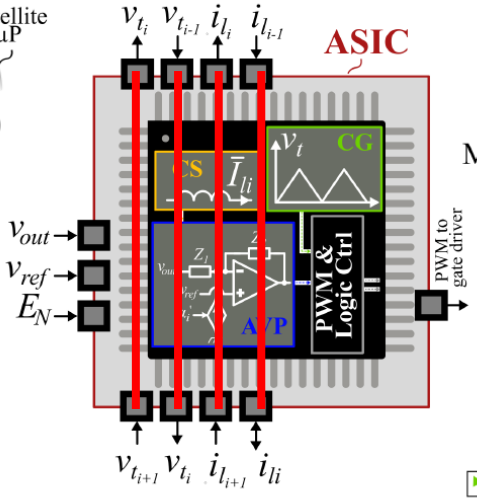
Fault tolerant & full operational Power Supply

Fully scalable

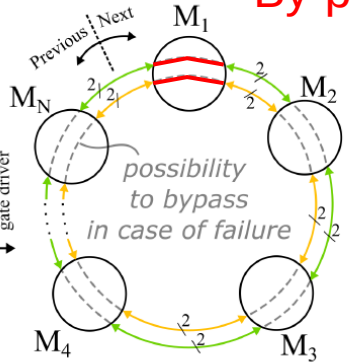
No supervisor required

Auto-reconfiguration (Fault-tolerant)





Main blocks as priority

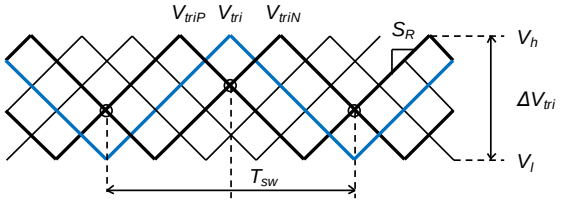


Funded by the European Union

2. MODELING – IMPLEMENTATION OF PROPOSED APPROACH

#1 – Interleaved Carrier Generation (CG) Block

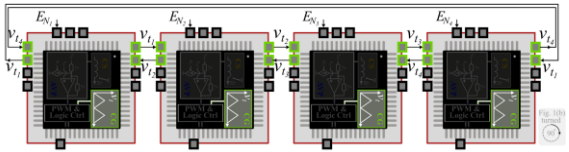
Principle of auto-interleaved Carrier Generation



$$\phi_{\Delta t} = \underbrace{\phi_{i+1}}_{\text{next}} - \phi_i = \phi_i - \underbrace{\phi_{i-1}}_{\text{prev.}} = \frac{2\pi}{N}.$$

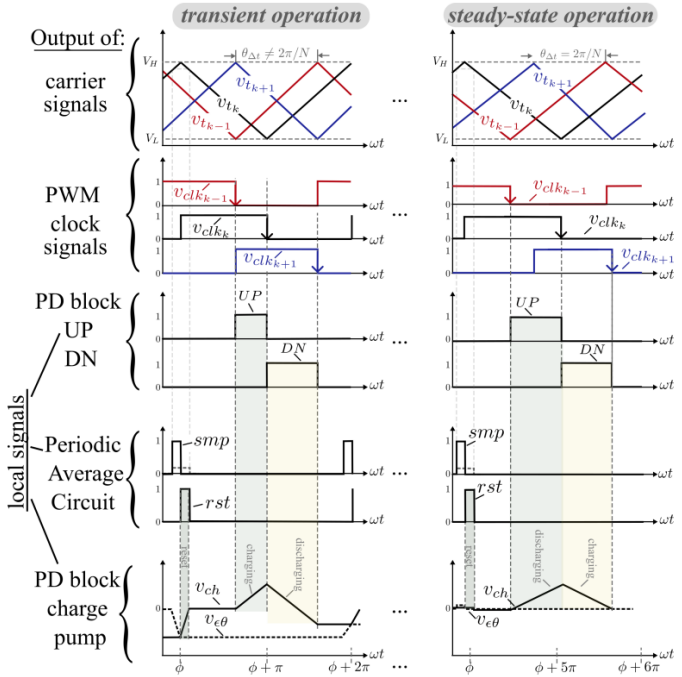
- We need to place each carrier rigorously at the center of next and previous carriers. So we need sure that:

A chain of Inter-ASIC communications.



Each ASIC exchanges information with its close neighbors

How does it works ?



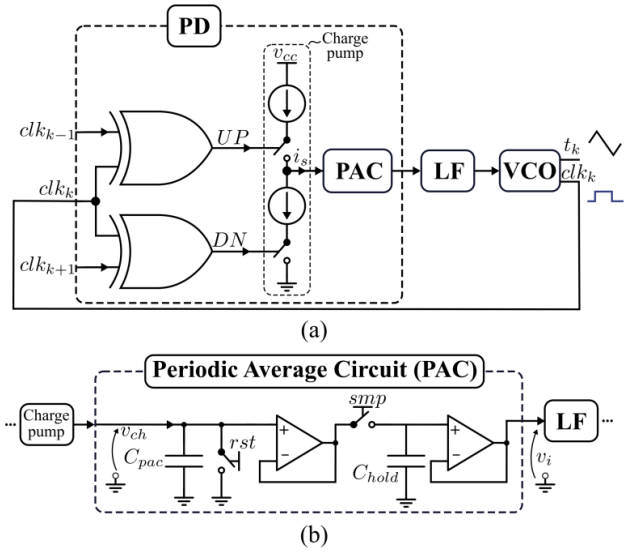
Generation of a relative position error signal

Funded by the European Union

2. MODELING – IMPLEMENTATION OF PROPOSED APPROACH

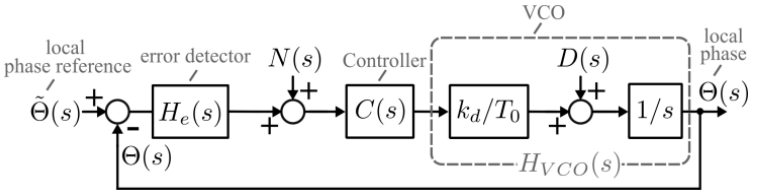
#1 – Interleaved Carrier Generation (CG) Block

Implementation : a 2-inputs PLL circuit



2I-PLL overview for local k-th module example.
(a) PD block. (b) PAC block

Low-pass filter and stability concerns



Control block diagram of a single-loop representing one LC elements.

$$\tilde{\Theta}(s) = \frac{1}{2}\underbrace{\Theta_{k+1}(s)}_{\text{next}} + \frac{1}{2}\underbrace{\Theta_{k-1}(s)}_{\text{previous}}$$

$$H_e(s) = \underbrace{e^{-s.(T_0/2)}}_{H_{delay}(s)} \cdot \underbrace{\frac{1-e^{-s.(T_0)}}{s.(T_0)}}_{H_{ZOH}(s)} \cdot \underbrace{\frac{2.I_p.T_0}{C_{rst}}}_{\text{charge pump}}$$

$$H_{VCO}(s) = \frac{1}{s}.\frac{k_d}{T_0}$$

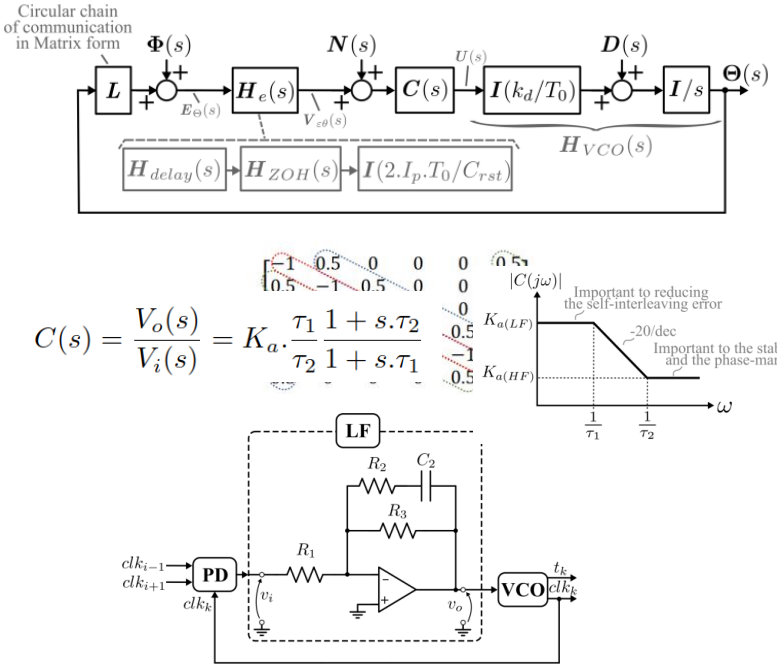
Generation of an relative position error signal

Funded by the European Union

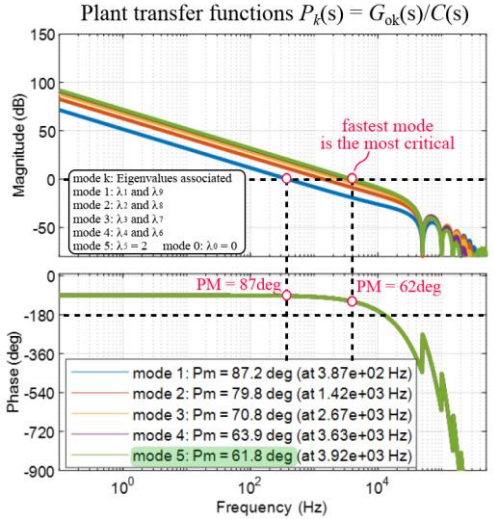
2. MODELING – IMPLEMENTATION OF PROPOSED APPROACH

#1 – Interleaved Carrier Generation (CG) Block

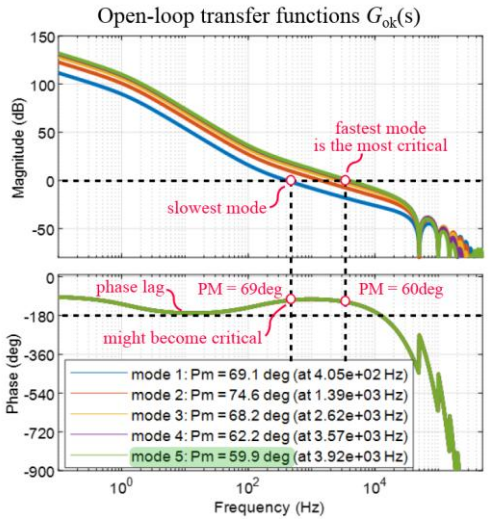
Corrector design and modal response



Modal response



Modal response with a simple proportional for C(s)



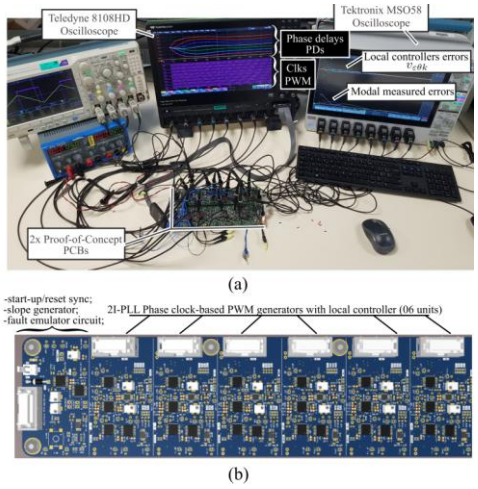
Modal response with C(s)

Funded by the European Union
imec embracing a better life
ISD Integrated Systems Development
SYNERGIE CAD PSC Partner SemiConductors
ThalesAlenia Space
ISD Aerospace Integrated Systems Development
TOULOUSE INP

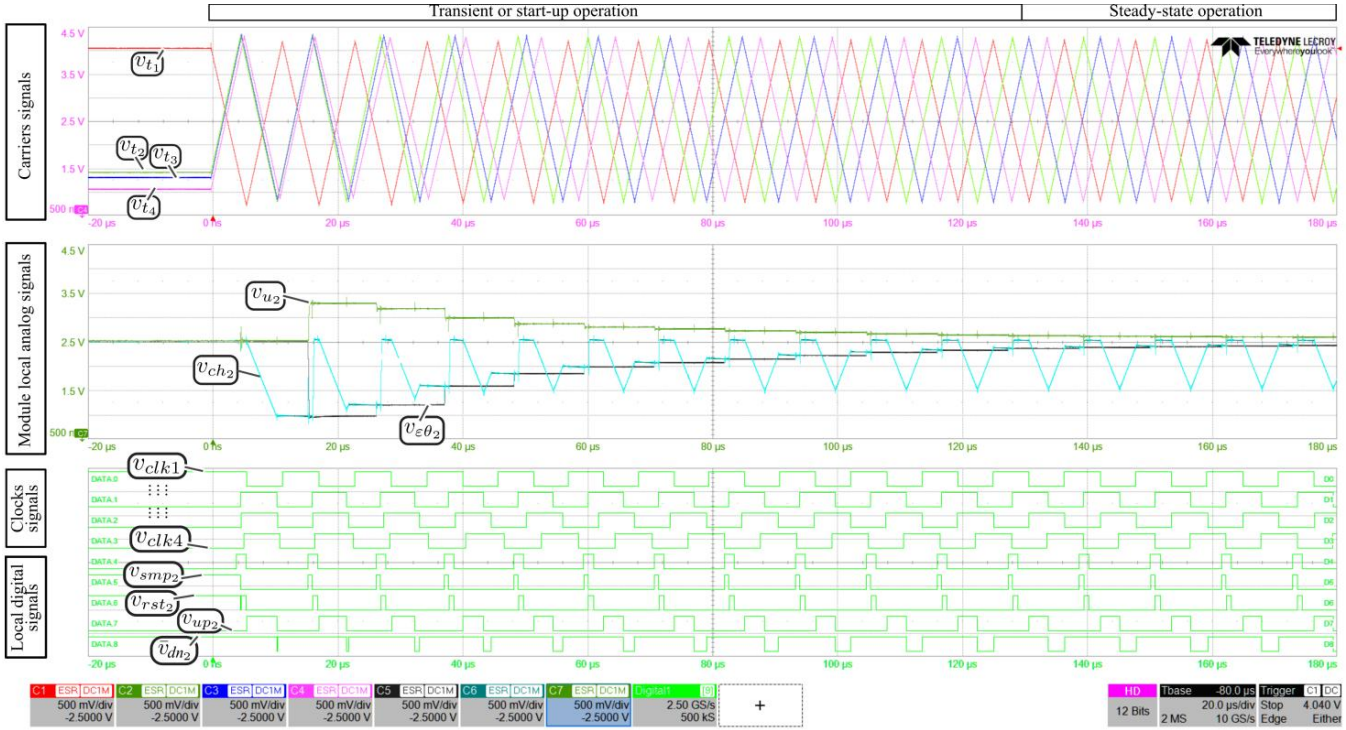
2. MODELING – IMPLEMENTATION OF PROPOSED APPROACH

#1 – Interleaved Carrier Generation (CG) Block

Experimental results



Experimental results. (a) Set-up overview. (b) Proof-of-concept board with 6 local controller boards and shared functions.

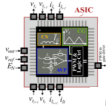


Funded by the European Union

2. MODELING – IMPLEMENTATION OF PROPOSED APPROACH

#2 – Adaptive Voltage Positioning (AVP) Block

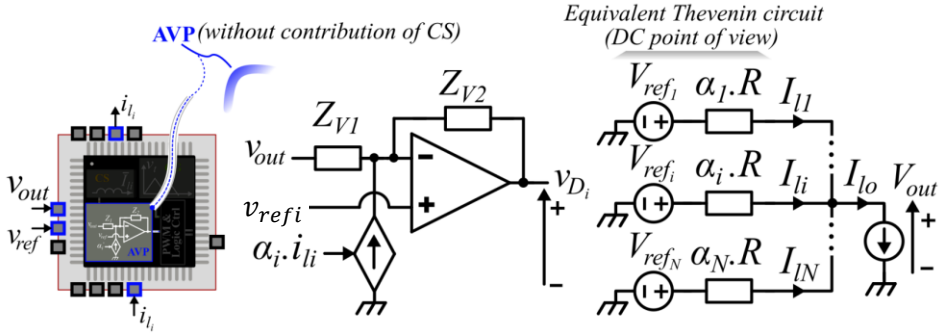
Decentralized AVP Principle



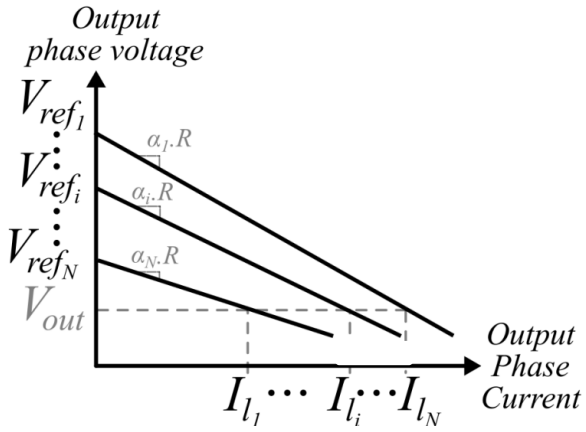
- Each module determines its own duty-cycle
- A drop control method is used

$$V_{out} = V_{ref_i} - \alpha_i.R.I_{l_i},$$

Local voltage reference — Drop control



Output characteristic (load-line or droop or drop)



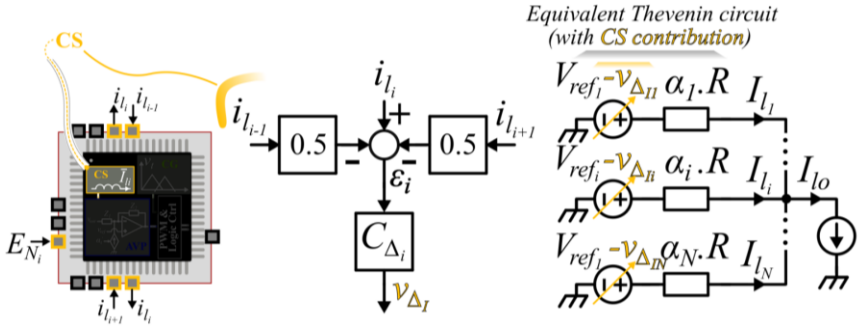
- Mismatches between modules must be considered
- Resulting in unbalanced currents

Funded by the European Union

2. MODELING – IMPLEMENTATION OF PROPOSED APPROACH

#3 – Current-sharing (CS) Block

Principle of Current-sharing

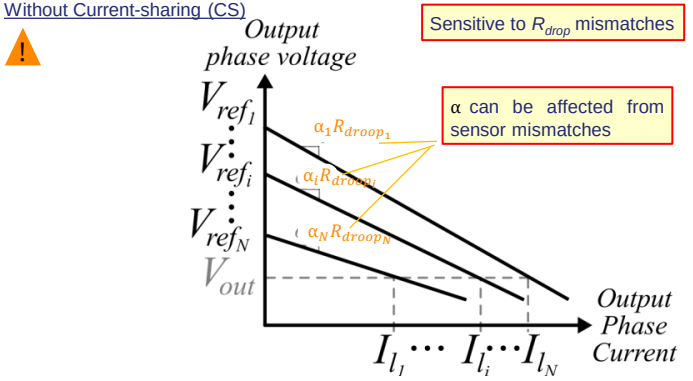


$$e_i(t) = i_{l_i}(t) - 0.5(\underbrace{i_{l_{i+1}}}_{\text{next}}(t) - \underbrace{i_{l_{i-1}}}_{\text{prev.}}); \qquad C_{\Delta_i}(s) = \frac{V_{\Delta_{Ii}}(s)}{E_i(s)} = \underbrace{-K_{\Delta i}}_{\text{Closed-loop time response}}\left(\frac{1}{1+\underbrace{\tau_{\Delta i}.s}_{\text{Tuned to guarantee system stability}}}\right)$$

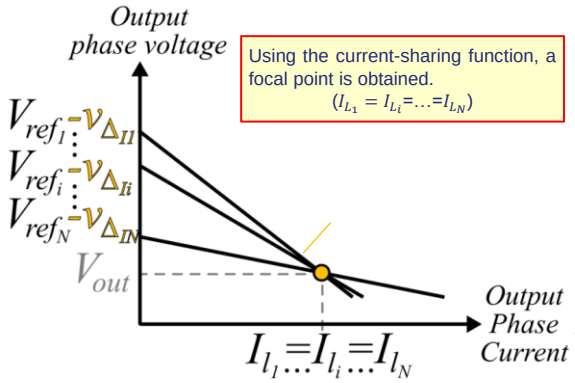
- The CS function is decentralized.
- CS functions balance the phase currents by adjusting the relative position of the characteristics.
- Thanks to the ring communication, it becomes easy to remove a module from the chain.

Phase current balacing

Without Current-sharing (CS)



With Current-sharing (CS)

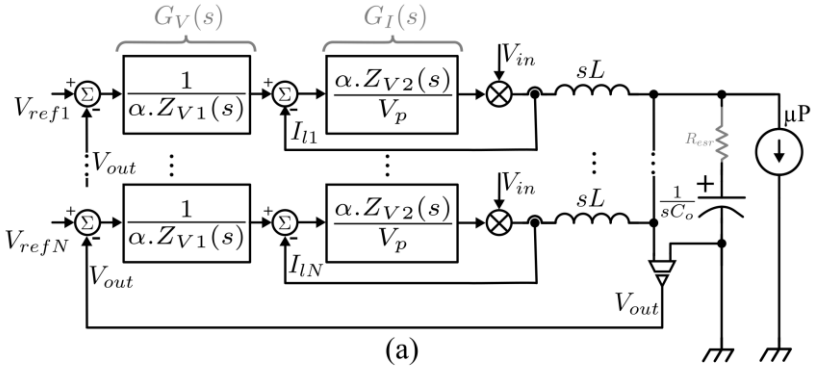


3. DISCUSSIONS – ANALYSIS AND SIMULATION RESULTS

#Design and Stability Analysis

Controller Designs

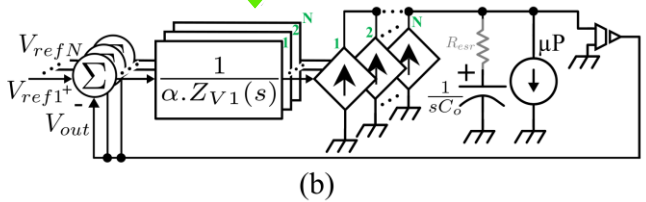
AVP control block diagram for N-modules



Simplified circuit

$Z_{V1}(s) = R_{V1}$, and
$Z_{V2}(s) = R_{V2} + \frac{1}{sC_{V2}}$

Simplification
For $f_{cI} \gg f_{cV}$

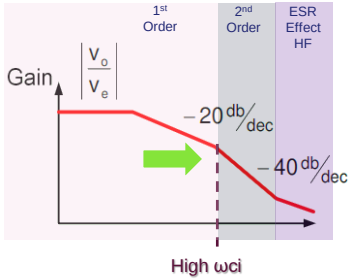


- A high **ωci** can **simplify** the buck converter from a 2nd-order system to a 1st-order system (i.e., the inductor becomes a voltage-controlled current source).

$$R_{V1} = \frac{1}{\alpha}.\frac{\Delta V}{I_{L_{Max}}};$$

$$f_{cV} = \frac{1}{2\pi}.\frac{1}{\alpha R_{V1}}.\frac{N}{C_o},$$

$$f_{cI} = \frac{1}{2\pi}.\frac{V_{in}}{V_p}.\frac{\alpha R_{V2}}{L},$$



Expected open-loop transfer function

- Frequency relationship and Guidelines. Make sure to

$\omega_{sw} >> \omega_{cTi} >> \omega_{cT2}$
$\omega_{cTi} = 0.33\omega_{sw}$ and $\omega_{cTv} = 0.1\omega_{sw}$

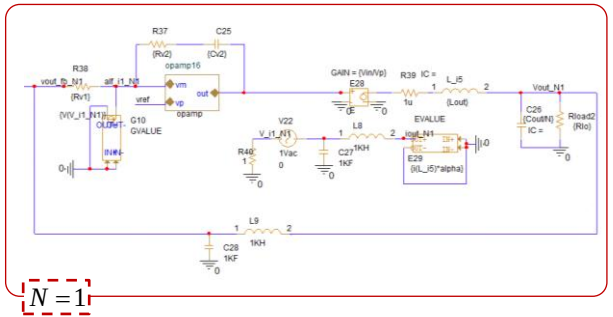
$$f_{cI} = \frac{1}{3}f_{sw}; \qquad f_{cV} = \frac{1}{10}f_{sw};$$

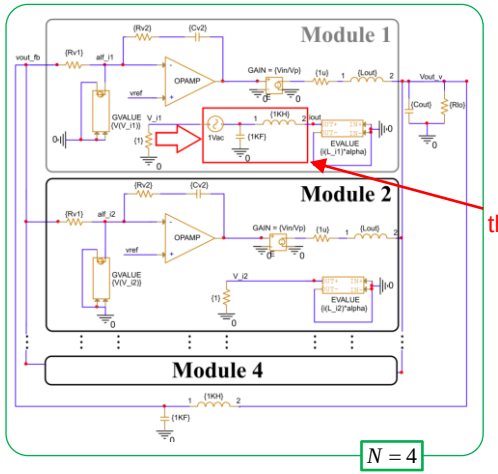
Funded by the European Union

3. DISCUSSIONS – ANALYSIS AND SIMULATION RESULTS

Simulation results (Frequency-domain)

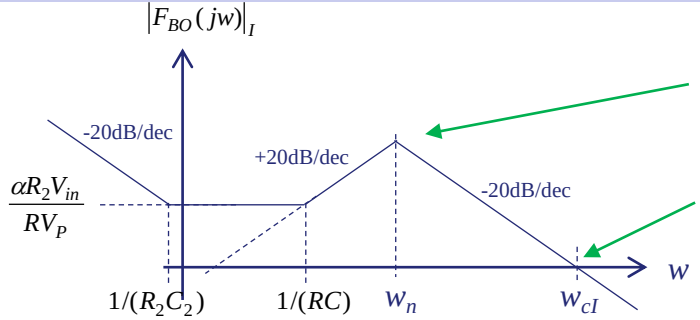
- Impact of *N* in the current loop (Inner loop)



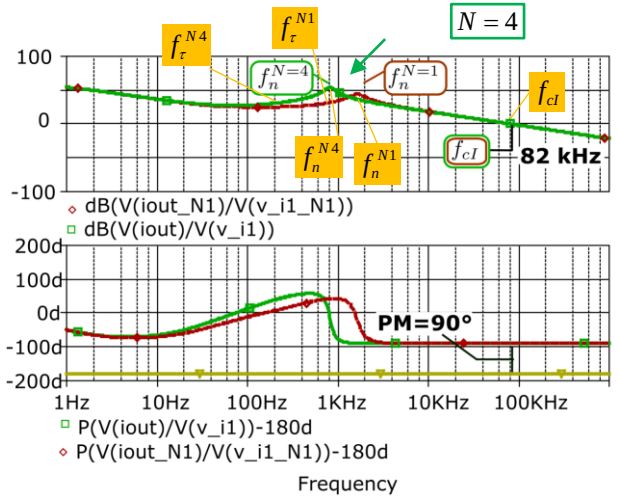


[Opening the inner-loop]

Theoretical Transfer Function



Inner-loop



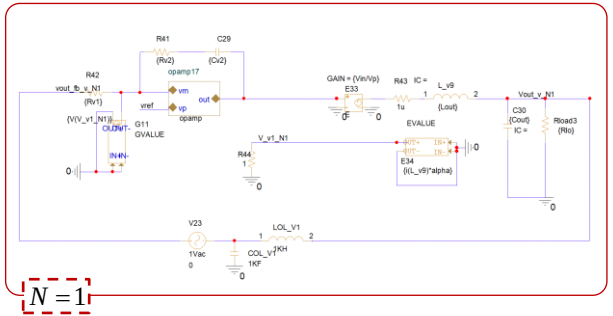
Note:

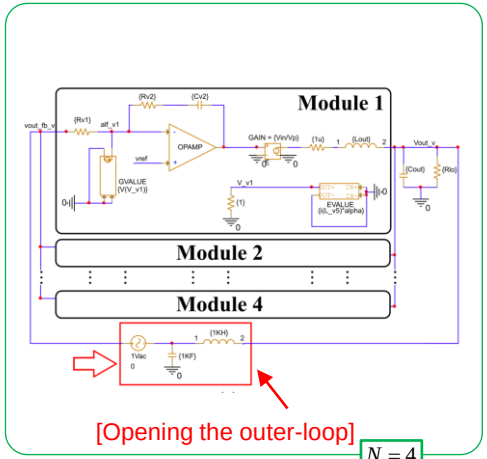
- There is no change in current loop bandwidth
- f_n^N variation is lower than f_τ with N variation
- f_n^N and f_τ change as long as *N* and C_{out} changes
- Open-loop Unconditionally stable

3. DISCUSSIONS – ANALYSIS AND SIMULATION RESULTS

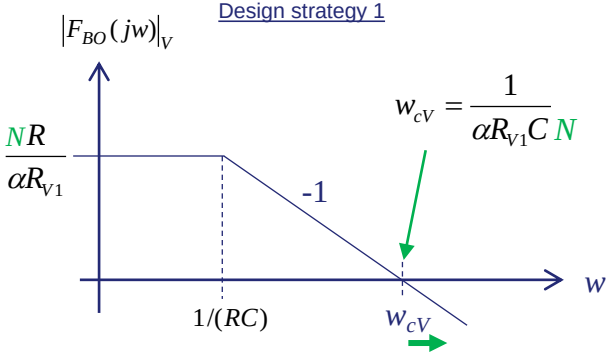
Simulation results (Frequency-domain)

- Impact of *N* in the voltage loop (Outer-loop)



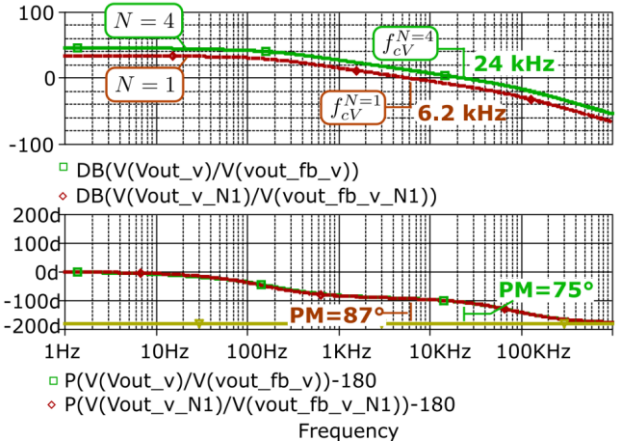


Theoretical Transfer Function



Outer-loop

Design strategy 1

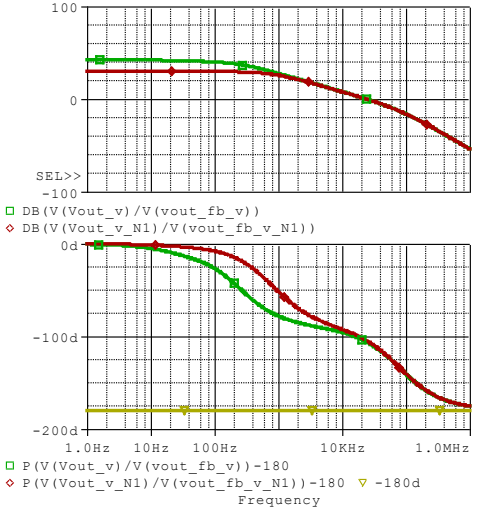


Outer-loop with normalized C_o'

Design strategy 2

If C_o value is normalized as $C_o' = C_o/N$ in one-module there is no change in HF

$$f_{cV} = \frac{1}{2\pi}.\frac{1}{\alpha R_{V1}}.\frac{N}{N.C_o'} = \frac{1}{2\pi}.\frac{1}{\alpha R_{V1}}.\frac{1}{C_o'}$$

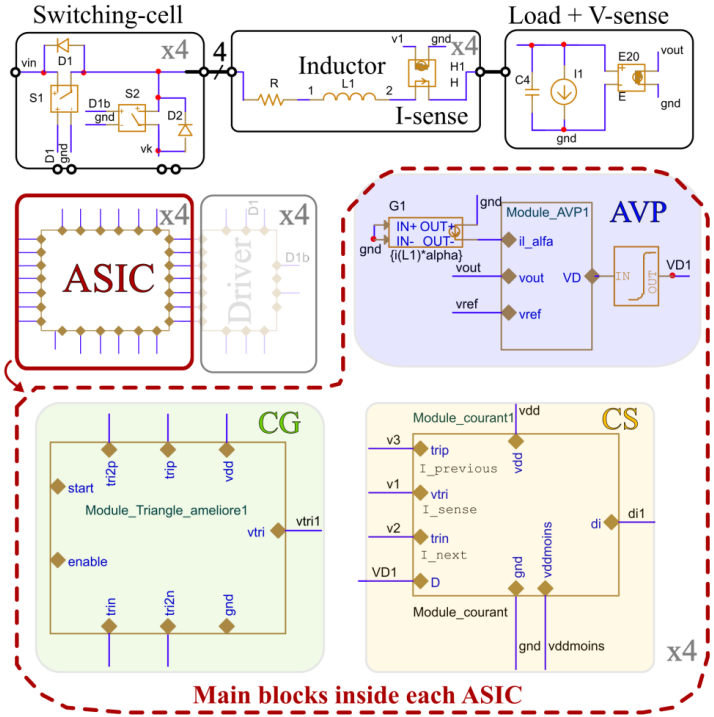


3. DISCUSSIONS – ANALYSIS AND SIMULATION RESULTS

Simulation results (Time-domain)

MAIN SPECIFICATIONS FOR SIMULATION TESTS OF THE SYSTEM.

Parameters	Value	Description
f_{sw}	250 kHz	Switching frequency
N	4	Number of Phases
I_{out}	40 - 100 A	Output current range
I_{ph}	10 - 25 A	Phase current range
V_{out}	0.6 - 1.2 V	Output voltage range
V_{in}	3 - 12 V	Input voltage range
$\Delta_{V_{max}}$	30 mV	Maximum admissible output voltage range
α	0.01 m	Effective current sensor sensitivity
R_{V1}	100 Ω	AVP-Controller $Z_{V1}(s)$
R_{V2}	19.6 kΩ	AVP-Controller $Z_{V2}(s)$
C_{V2}	50 nF	AVP-Controller $Z_{V2}(s)$
αR_{V1}	1 mV/A	AVP Slope per phase



Funded by the European Union

3. DISCUSSIONS – ANALYSIS AND SIMULATION RESULTS

Simulation results (Time-domain)

❑ Steady State Result

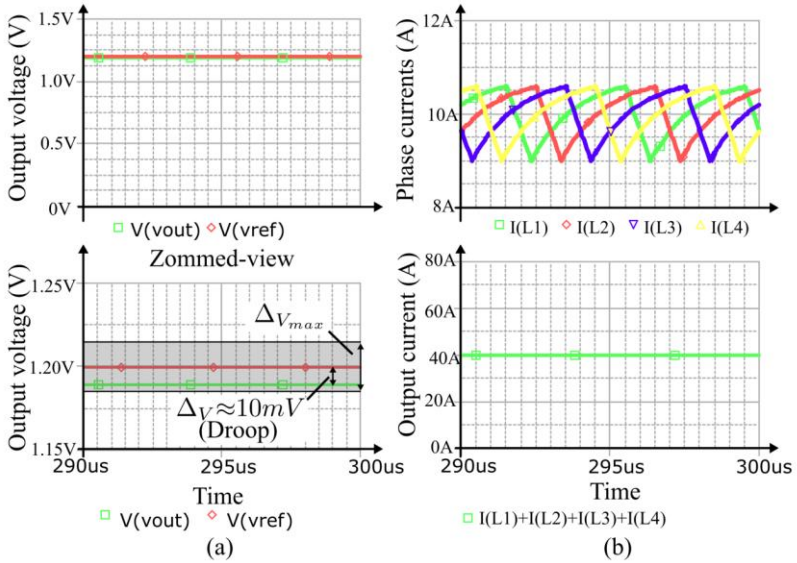
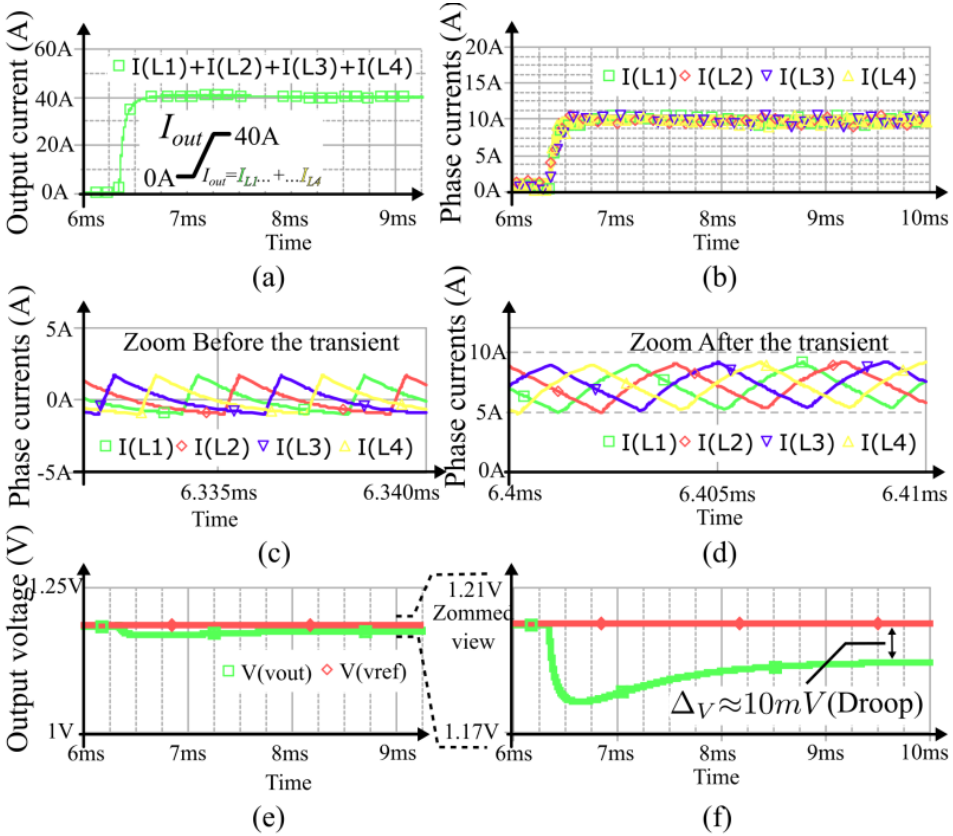


Fig. 10. Simulation result. Steady-state waveforms. (a) Output voltage. (b) Phase currents (on the top) and Output current (on the bottom).

❑ Load Transient Result

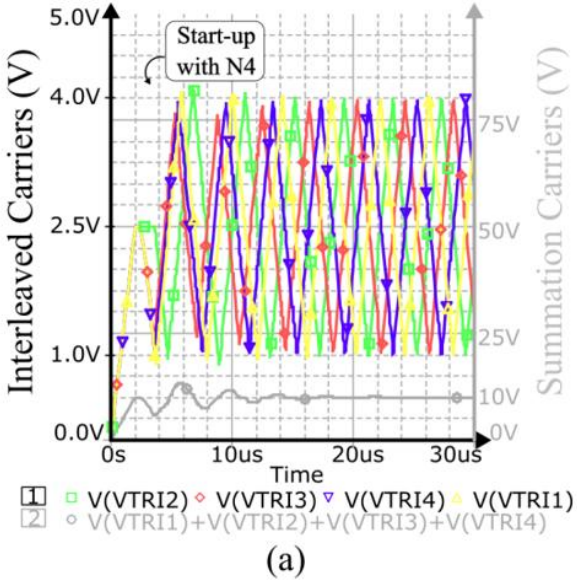


Funded by the European Union

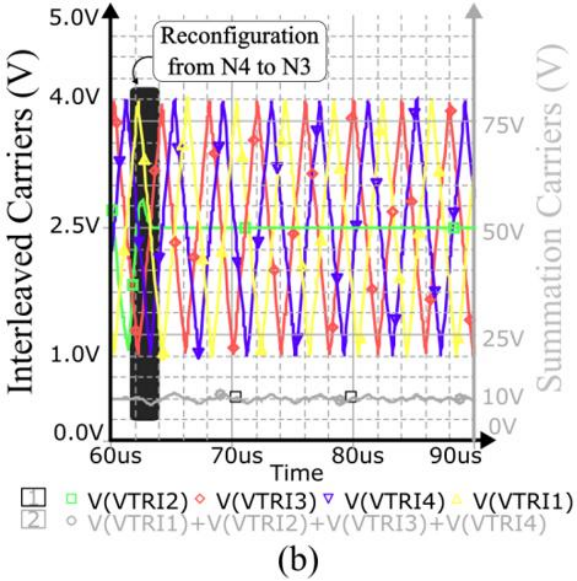
3. DISCUSSIONS – ANALYSIS AND SIMULATION RESULTS

Simulation results (Time-domain)

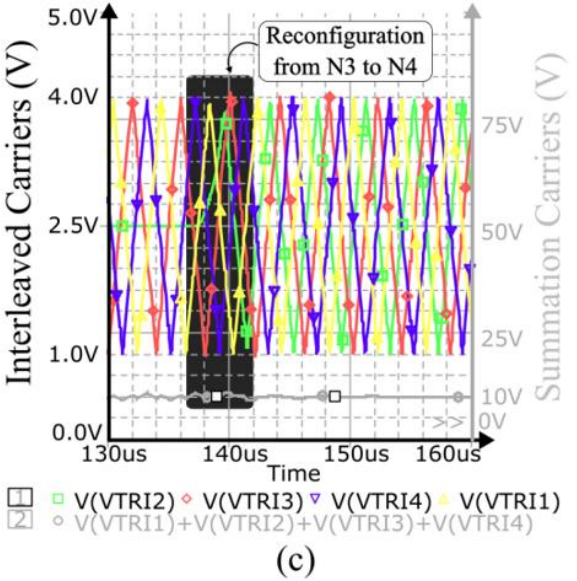
- CG Block simulation with reconfiguration test



Experimental setup. (a) Start-up



(b) Reconfiguration from 4 to 3 phases

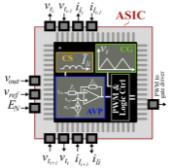


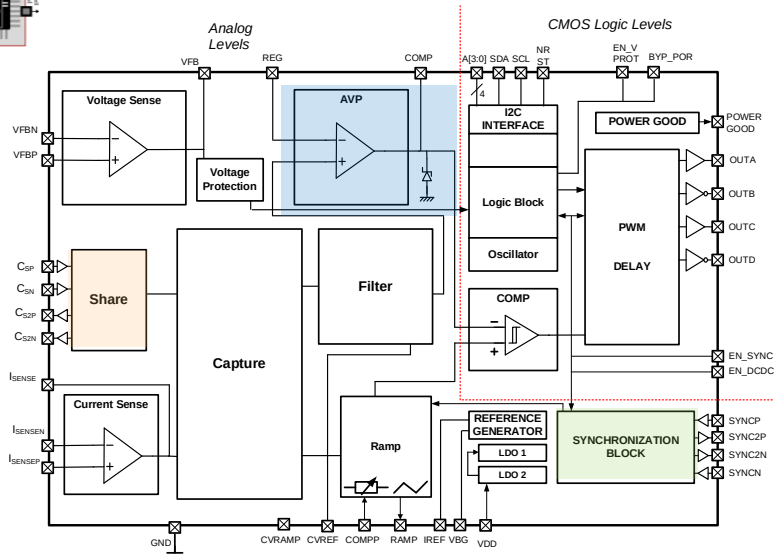
(c) Reconfiguration from 3 to 4 phases

Funded by the European Union

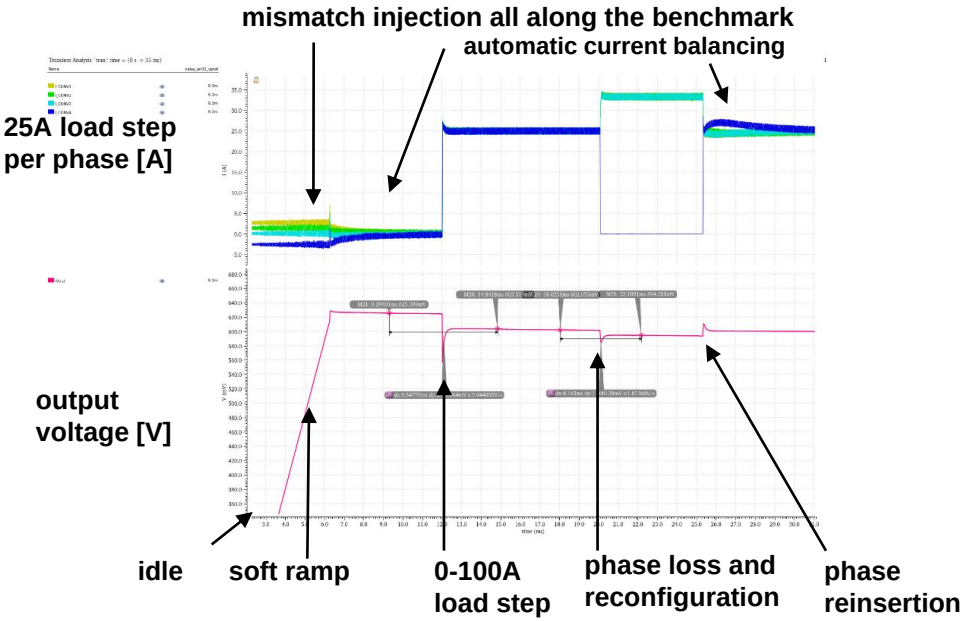
3. ANALOG BEHAVIORAL MODELING AND IMPLEMENTATION

- ✓ Prior to the ASIC design phase, a detailed model was developed at sub-block level which allowed :
  - the validation of the system architecture down to individual functions
  - the debugging and correction of some design hypothesis





ASIC top architecture



Simulation example for a 4-controller 100 Amperes configuration

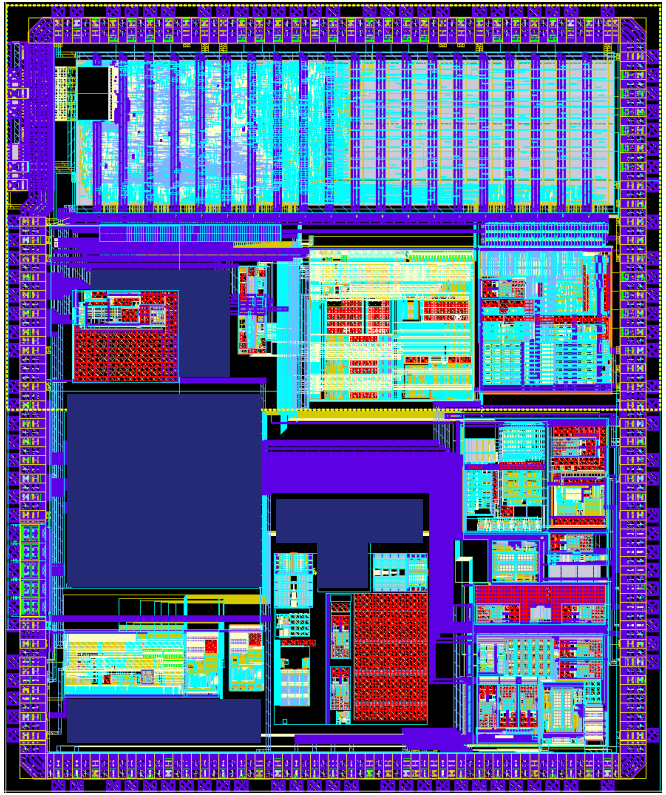
Funded by the European Union

4. ASIC HARDENING FOR SPACE

- the digital control functions are developed using a design methodology to guarantee the good function over the mission profile with :
  - ✓ radiation hardened standard cells library
  - ✓ auto corrective registers, especially the control of the analog part.
  - ✓ lock free state machines (prevent loss of functionality due to register upset or SEFI)
  - ✓ system resilient to unexpected reset with a transparent reinsertion of a circuit.

- At system level, mismatch and events were injected during the simulations to harden the analog part to the right need (no excess design nor underdesign), especially for :
  - ✓ current sensing and sharing with other circuits.
  - ✓ voltage sensing and adaptive voltage positioning.
  - ✓ pulse with modulation with non overlapping outputs by design
  - ✓ inter-circuit synchronization or standalone operation.
  - ✓ integration of electrical constraints of large PCBs.

- At top level, mixed signal simulations (digital RTL code + analog at transistor level) to guarantee the right control, connections, and generate test patterns for industrialization.



ASIC Layout (X-Fab 180nm XH018, 5x6 mm²)

Funded by the European Union

4. CONCLUSIONS AND FUTURES WORKS

Conclusions

- A decentralized control concept applied to a multiphase interleaved synchronous buck converter suitable for power management in satellites systems has been presented.
- Three main features of each local ASIC: i) the self-interleaved carriers/PWM signals, ii) Local AVP voltage regulation, iii) and local the current-sharing capability.
- Possibility to improve system functional safety thanks to:
  - **Modularity and Scalability**
  - **Fault-tolerance and auto-reconfiguration capability** (operation with N-1 active phases is guaranteed under a faulty condition).
  - **Local controllers connected in a circular chain of communications**.
- The proposed method and theoretical expectations are validated by SPICE simulations and lab. prototypes,

Funded by the European Union

ACKNOWLEDGMENT

- This project has received funding from the European Union's Horizon Europe research and innovation program under grant agreement No 101082266.

- The authors acknowledge the active contribution of
  - Thales Alenia Space,
  - LAPLACE laboratory, Institut National Polytechnique de Toulouse (INP-Toulouse),
  - ISD,
  - Synergie CAD,
  - and IMEC.

THANK YOU

Visit our website for more: https://scopsproject.eu/

Funded by the European Union