Radiation Hardened by Design SONOS embedded Non-Volatile Memory in 180nm

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***Abstract*— In this article we report about a design of new mixed-signal embedded non-volatile memory (eNVM) IP in 180nm technology with high voltage (HV) and silicon–oxide–nitride–oxide–silicon (SONOS) design solutions, together with and hardening against radiation effects. The purpose is to create an eNVM solution for space applications. The design is in the final completion stage and the test vehicle design is due to be sent to manufacturing soon. The main specifications of the IP are memory size 256x64 of 32-bit words, clock frequency 16MHz (+/-10%), power supply 1.8V/3.3V, area 21.15mm2. The IP consists of three main parts: digital controller, full custom memory core and high voltage control with third-party charge pump IP. This IP is within the scope of DARE180XH platform. The mission profile does not require the design solution to use HV operations such as program and erase. Thus, for regular operations the design boundaries were purely dictated by the mission requirements. Therefore, radiation hardening design efforts were concentrated on data safety (integrity) during read operations. To address the overall data integrity threats, error checking and correction (ECC) with data path scrubbing and scrambling/descrambling were implemented. Variable-speed read operation and triple read options were made available for the user to increase confidence in read safety. Degradation caused by total ionizing dose (TID) effects and general aging is mitigated by limited self-calibration techniques. Further immunity of the analogue circuitry against TID and latchup is preserved by layout design. For that purpose, special DRC were implemented. To improve read operations in harsh environment, especially at the end of life, configurable sense amplifiers were developed. For testability and functional safety, a design for test (DFT) approach was used. The digital memory controller was synthesized from RTL and was mapped to a radiation hardened standard cell library with DICE flip-flops and specially designed combinational cells for clock and reset signals single event transient (SET) hardening. Furthermore, all analogue and digital IP blocks were systematically scanned for SET sensitive nodes using an in-house tool and special testbenches. SET filters were added on all critical control signals to improve SEE behavior. The test vehicle containing this IP is expected to be taped out in Q2 2022. The characterization, irradiation and reliability tests will be applied to this test vehicle. Space-grade radiation hardened memory is expected to be ready for production in 2023.**

I. Introduction

This Design was initiated by one of the IMEC's partners, a large EU aerospace consortium. The basic specification required 42 to 64 portions of 256 words, 32 bits each. Out of the 32bits 8bits were used for ECC, the rest for bitstream. The eNVM Macro is an integral part of the field programmable gate array (FPGA) for aerospace application and will be used as configuration memory for the FPGA.

As an initial basis for this design third-party nvSRAM in 180nm technology was proposed. Therefore, the third-party charge pump IP was initially chosen for HV generation, as it was designed specifically for programming and erasing the SONOS memory cells. However, the nvSRAM array as such was prone to latch-ups, so IMEC has decided to go for a six-transistor bit cell flash architecture, Fig. 1. With this solution direct and inverted data are stored and are used with for differential sensing. Additionally, select top and select bottom transistors are deployed. The PAGE addressing scheme had to be changed completely too.

HV stress per page is limited to 1000 HV OPs only, as the eNVM is going to be programmed in the lab before the mission and subblocks for HV generation will be disconnected from the power supply in the mission to avoid latch-ups. The eNVM re-configuration will still be available if re-initialization is enabled in the eNVM config, which is also built in the memory array.

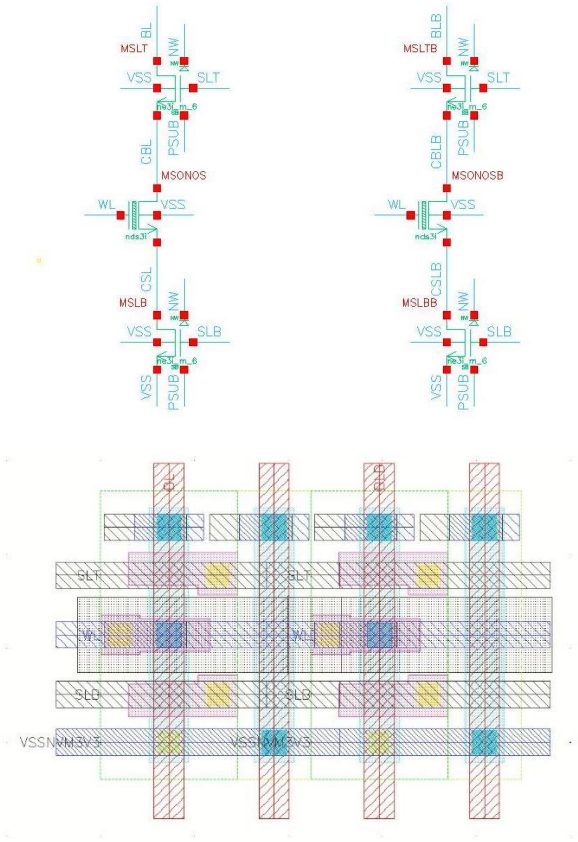

Fig. 1. Six transistor bit cell architecture schematic and layout

II. Main specifications of IMEC eNVM Macro

Memory core organization is presented on Fig. 2 and specified in the Table I along with operating conditions and electrical specifications. Splitting Array in two BANKs allows more even distribution of the memory cells, reduce load on the charge pump at high leakages, reduces probability of fail and improve timing by reducing so Bit Line parasitic capacitances. Each memory bank organization is depicted on Fig. 3.

eNVM macro has its own configurational and redundancy space in two additional SECTORs, which are separate ones in both Memory BANKs, Fig. 4. These are only partly available for the user. PAGEs 6 to 0 of these SECTORs are dedicated for eNVM CONFIG, and all information stored here in RAID 1 like type of storage, i.e., is mirrored in both BANK0 and BANK1 and employ ECC by default. Pages 31 to 16 are dedicated for PAGEs failed in the USER Volume. Once remapped, eNVM will always address the failed PAGE here. Each BANK has own dedicated REDUNDANCY space.

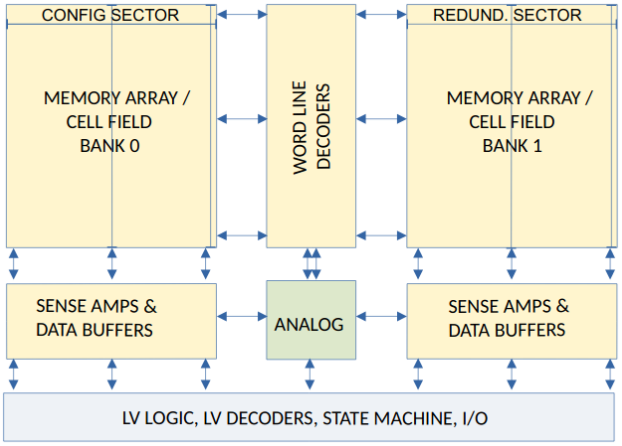

Fig. 2. Memory Core with Memory Periphery

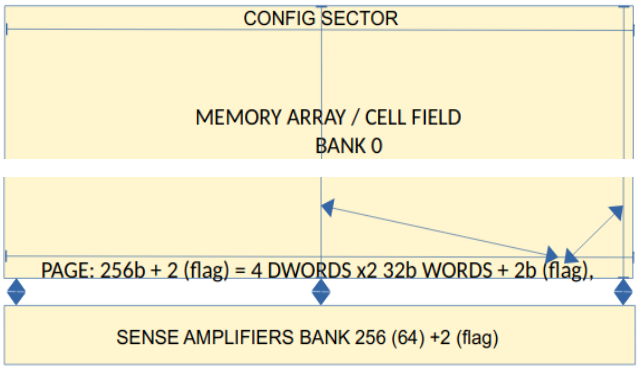

Fig. 3. Memory Bank, 256b per Page, 32 Pages per Sector, 32+1 Sectors

Table I. Memory Organization and Specifications

Memory Array		
1.1	Word, bits	32
1.2	Number of User Data Words	256x64
1.3	Additional Configuration Space, Words	256 (56 active)
1.4	Additional Redundancy Space, Words in Bank 0 and Bank 1	256
1.5	Page, Words	8 (+2 flag bits)
1.6	Pages per Sector	32
1.7	Sectors per Memory Bank	32+1 (CONFIG/ REDUNDANCY)
1.8	Memory banks	2
1.9	ECC Bytes per Page	8
1.10	ECC Bits per Word	8
1.11	Total Amount of Memory, User Volume + CONFIG/REDUNDANCY, bits	524288+16384
1.12	Sense amplifiers per Page	256 (+2 flag)
Synchronous Parallel User Interface (UI)		
2.1	Data I/O Width, bits	32 (+2 flag I/O)
2.2	Random Access Latency, Clock Cycles	3
2.3	Burst READ Latency, Clock Cycles	1
2.4	Single HV OP Latency without Remapping, ms	16
2.5	Longest HV OP Latency with Remapping, ms	80
2.6	CE high to OP wait, Clock Cycles	1
2.7	User SKIP INIT	yes
2.8	User Triple Read Option/SAFE READ	yes
2.9	INIT from User Source	yes
2.10	eNVM System Clock Frequency, MHz (external clock)	16 (+/-10%)
2.11	Address space	<12:0> + 2 bank enable bits
2.12	Separate safe access to the eNVM CONFIG, for READ + WRITE	CONFIG + TM UI signals
Recommended Operating Conditions and Electrical Specifications		
3.1	Power Domains, V	1.8, 3.3 (+/-10%)
3.2	Total Targeted Average Current Consumption in HV OP and READ, mA	<50mA
3.3	Total Targeted Average IDDQ Current Consumption, uA	<10uA
3.4	Operating Temperature, TA, oC	-40 … 125
3.5	Storage Temperature, TA, oC	-40 … 150
3.6	Data Retention, Years	10
Radiation Hardening Level		
4.1	Targeted Tolerance to TID, krad (Si)	100
4.2	Targeted Tolerance to SET, LET, MeV*cm2/mg (Si)	60

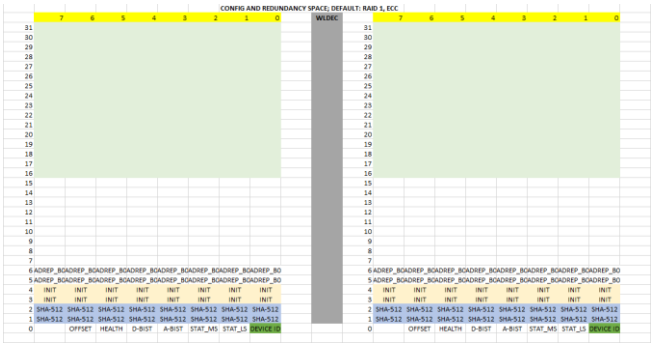

Fig. 4. 6:0 CONFIGURATION / 31:16 REDUNDANCY space (not User Volume, these are solely eNVM validation and setup sectors, no User information can be stored here), CONFIG is written in RAID 1 like mirroring, i.e. same data in both BANKs, whereas REDUNDANCY is specific for each BANK. Physical placement, axis X: WORDS (8 per PAGE), Y: 32 PAGES, 15:7 not used now

III. DESIGN FOCUS

HV OPs (operations) will be disabled during the mission. Therefore, key focuses were put on hardening of READ Operation, eNVM INIT OP, Test Modes and the overall Safety and Integrity of the Data.

Besides mapping digital eNVM controller to the special libraries, multiple original algorithms of Data protection and recovery were implemented in the eNVM controller. Meanwhile, in the full custom part architectural, design and layout measures were taken to reduce sensitivity against specified TID and SEE.

In order to address degradation of programmed and erased thresholds of SONOS memory cells caused by aging in general and/or by collected dose, a special Sense Amplifier (SA) architecture was developed. It allows five READ modes of the Sense Amplifier – three differential and two pseudo single-ended modes with self-biasing and mismatch sampling.

The user may configure the SA itself by writing eNVM CONFIG respectively before the mission. Alternatively, the SA can be configured during the mission by overwriting eNVM controller INIT registers, choosing between differential sensing and one-sided sensing, so-called pseudo single-ended mode, sensing either the Bitline (BL) or the inverted Bitline (BLB).

If enabled in the eNVM CONFIG space, a special self-calibration algorithm kicks in after every RESET. The algorithm then sweeps operational modes of Sense Amplifiers, adapting READ OP to the memory cell current degradation also by searching for suitable Bitline reference currents and VREAD voltage. Additionally, trimming of the SA control signals timings is done to oppose degradation within the digital eNVM controller and SA.

To reduce READ disturb and to speed up READ out, whole page is buffered in one RANDOM ACCESS into Data Out Shadow Buffer and then Data are read out from that Shadow Buffer. The whole User Volume can be read out in such a Burst READ when read out approaches WORD<6> of the current PAGE, next PAGE gets buffered, eliminating so random access READ latency.

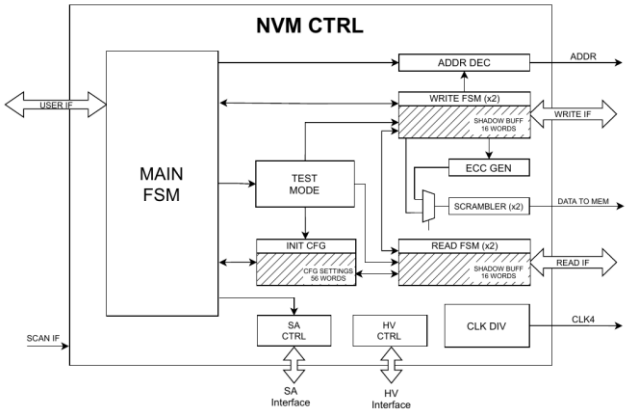

Fig. 5. Digital eNVM controller integrates multiple FSMs for User Mode and Test Mode OPs and has four Interfaces: UI, TI, CP IP and SCAN

Error correction can be applied in a built-in scrubbing loop right in front of the Data Out multiplexer in the UI, covering so most of the Data Out path and respectively any potential data corruption cumulated by all elements of that DO path.

To reduce sensitivity to the SET Data Path scrambling/descrambling is implemented along with internal Error Correction – thus, a charged particle will never corrupt more than one bit per WORD. The user may also skip address comparison and re-READ from the physically addressed PAGE, i.e., from the memory cell again and again, e.g. for triple random access READ.

In order to further increase safety of data storage, RAID 1 type of storage is available for the user when enabled in eNVM CONFIG. In this case, the user may mirror Data in both memory Array Banks and detect and correct twice as many Errors.

A Data Integrity Check feature is also incorporated in every WRITE. Here FSM acquires data at the UI, stores it in the Data In Shadow Buffer and then writes it into the SA, then reads SA out to the Data Out Shadow Buffer and compares both buffers.

WRITE Operations have optional WRITE VERIFY which is READ OP performed 1ms after WRITE is over. This can be activated in the eNVM CONFIG and will run seamlessly, but the user will be informed about the result via flag bits at the UI. Additionally, the user may also enable automatic REDUNDANCY mapping. In this case, the algorithm will initiate WRITE, WRITE VERIFY, if not successful, then WRITE and VERIFY again, if not successful then remap failing PAGE to another PAGE within REDUNDANCY space in the BANK.

ERASE one PAGE is per hardcoded in the third-party CP IP internal FSM essentially just WRITE all zeroes. Only one sequence is hardcoded in the CP IP FSM which is PRE-PULSE→ERASE→PROGRAM, so ERASE is already incorporated in every WRITE OP, Fig. 6.

ERASE ALL to erase the entire User Volume is not verifiable and is just data shredding. Although it is available for the user, as such it only makes sense when the user wants to shred all the data at once.

Table II. Available automated or semi-automated Test Modes coded by UI adrress A18_I<12:0>. DFT is independent and is invoked separately

TYPE	ADDR	TM	TM NAME	COMMENT	FAIL CRITERIA
ANALOG	0	TM00	Virgin State to Normal	Few HV OPs: WRITE FF, ERASE ALL, then WRITE code for self-cal. in CONFIG. Doesn't need USER inputs	N.A.
	1	TM01	Self-Calibration	Algo looks up for error-free READ trim settings between two RESET sessions. Doesn't need USER inputs	NON-ERROR FREE READ
	2	TM02	IDDQ	Measure VDD* current upon sequential analog block-by-block deactivation	>200uA, all sources
	3	TM03	RUN TM0+TM1	Wafer Level Test Inclusion (possible)	See TM00 and TM01
	4	TM04	WL Leakage Test	Activate WL Leakage DAC/Comparator, as long as APSB is asserted, the test will run incrementally	>2uA leakage at RT
	5	TM05	SA Test	Running through Modes of SA OP, DIFF to Single Ended, RAID 1. No ECC is involved.	NON-ERROR-FREE READ
	6	TM06	Cell Margin & BL Leakage Test	Activate BL reference current, read out SA. For Cell Margin: set address, sweep VREAD, IBLREF	>2uA leakage at RT
	7	TM07	Aux Charge Pumps Test	Duty Cycle Measurement to track the auxiliary charge pump load, leakages. Doesn't need USER inputs	soft FAIL: >40%, hard FAIL: >90%
	8	TM08	Switch to EXTERNAL VREAD	Reconfigures internal MUX to accept externally fed VREAD, VBG, IBG for Cell Margins measurements	See TM00 - TM08
DIGITAL	9	TM09	Special Registers Read Out	All internal Registers, incl. Controller CONFIG, Device ID, REDMAP - all <6:0> CONFIG PAGES	N.A.
	10	TM10	REINIT from User source	16 WORDs only (READ CONFIG PAGE 3 and 4 contents in the FSM registers), VOLATILE only	N.A.
	11	TM11	REINIT from CFG	RE-READ CONFIG cpace of eNVM into eNVM FSM registers	FAILED FLAGS
	12	TM12	DI->SBI->SA->SBO->DO	Test for Data traverse: USER writes DI18_I, algo checks both DI & DO shadow buffers & SA	WRONG DATA
		DFT	DFT	Invoked independently from these addressed test modes	TBD

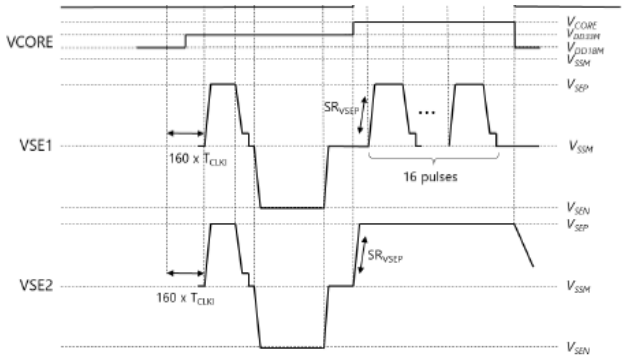

Fig. 6. Hardcoded HV OP sequence of the Third-Party CP IP (VSE2 changed on request of IMEC)

IV. Design For Manufacturability, Design For Yield and Testability

In order to make silicon validation easier and to pre-develop the production test program, be it wafer level or packaged chip level, 12 special Test Modes were developed and SCAN was addded too, all integrated into the digital eNVM controller, Table II.

Some of the test modes are fully automatic and require only start and logging on the tester side, thus saving testing time and efforts for coding/debugging during the production test development. This equally applies during initial Silicon Validation and/or for Failure Analysis, should that be needed.

In some of that test modes or their combinations some fabrication issues can be detected, design weaknesses sorted apart from that fabrication issues, general common aging effects, as well as collected TID induced effects can be assessed. In some cases this tests will help to increase yield when the user will interpret from their results and compensate some weaknesses with built-in current, voltage and timing reserves.

V. Conclusion

We set an ambitious goal to create an eNVM IP which, thanks to additional algorithms and built-in mechanisms, would adapt to and survive in harsh conditions. Both analog and digital design incorporates a relatively high grade of flexibility, safety, manufacturability and certain innovation. This was all achieved in a short timescale with very limited resources and all from scratch. We had no reference from previous products with the exception of the CP IP. Additionally, the constellation of the hardened memory array layout was developed from scratch.

We do understand that the risk due to added sophistication and complexity being high. On the other hand, we had to respond to challenges we faced in the course of the design and to compensate uncertainties, be it absence of statistical basis from the process or absence of leverage from previous products. We believe that only necessary complexity was added to our design to ensure efficient learning curve and fast silicon ramp up. We have done our utmost to develop and verify this IP to be ready for integration into the Pilot Circuit in a reasonable timescale and with improved device validation and test development always in consideration.

This eNVM IP has good potential to become a universal platform which can be reused in future projects along with reuse of gained experience, developed algorithms and sub-circuits. Third Party Charge Pump IP can be substituted by already built-in auxiliary Charge Pumps after their successful characterization and respective adjustment of the digital eNVM controller.

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