PROMISE

WP1 IPs Library and Pilot Circuit Specification

D1.3 Interface Standards & IP Usage Definition

Written by	***Responsibility*** + handwritten signature if no electronic workflow tool
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CHANGE RECORDS

ISSUE	DATE	§ CHANGE RECORDS	AUTHOR
001	16/03/2020	Document creation	G. Franciscatto
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LISTE DES OBJETS

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1. INTRODUCTION

1.1. SCOPE AND PURPOSE

This document contains the specification of the different interfaces and documents to be used in the IP delivery in order to guarantee the cross-compatibility of the IPs as well as compatibility with the common PROMISE design flow. The usage of the IP views within the design flow will be indicated.

1.2. APPLICABLE DOCUMENTS

None

1.3. REFERENCE DOCUMENTS

Internal code / DRL	Reference	Title	Location of record
RD1	IPP 1 3.0	Virtual Component Identification Physical Tagging Standard	http://vsia.org/docs/IPP_Tagging_Std%201_30.pdf

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1.4. DEFINITIONS AND ACRONYMS

ADC	Analog-to-Digital Converter
ASIC	Application Specific Integrated Circuit
CDL	Circuit Description Language
CDF	Component Description Format
DARE	Design Against Radiation Effects
DB	Database
DEF	Design Exchange Format
DRC	Design Rule Check
GDSII	Graphic Design System II
HDL	Hardware Description Language
HTML	HyperText Markup Language
I/O	Input/Output
IBIS	Input/Output Buffer Information Specification
IP	Intellectual Property
LEF	Library Exchange Format
LPE	Layout Parameter Extraction
LVS	Layout Versus Schematic
NDA	Non-Disclosure Agreement
OA	OpenAccess
PDF	Portable Document Format
PEX	Parasitic Extraction
PVS	Physical Verification System
RAD	Radiation Design
RTL	Register-Transfer Level
SDC	Synopsys Design Contraint
SDF	Standard Delay File
SPEF	Standard Parasitic Exchange Format
SVRF	Standard Verification Rules Format
VHDL	Very High-level Design Language
VITAL	VHDL Initiative Towards ASIC Libraries
VSIA	Virtual Socket Interface Alliance

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1.5. DOCUMENT OUTLINE

Section 1 describes the purpose, scope and application field of this document. In addition, it gives useful information for a better understanding of the document such as applicable documents, reference documents, specific definitions used or refer to in the document and at least the list of acronyms used. A brief presentation of its content completes this section

Section 2 describes IP deliverable views and package standard structure to be adopted by all IP providers in the context of PROMISE project.

Section 3 describes minimum validation steps to be performed on IP deliverables upon release.

Section 4 describes the use of deliverable IP views in analog-on-top and digital-on-top design flows as well as their application in the design of mixed-signal applications.

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2. IP DELIVERABLES [IPDE]

Requirement IS-IPDE-01 :

IP deliverables refer to the set of library or IP views provided by any partner design house.

[vmethod: Analysis]

Requirement IS-IPDE-02 :

IP deliverable data will be distributed in tarball compressed package files containing views and documentation arranged in a predefined directory structure.

[vmethod: Analysys]

Requirement IS-IPDE-03 :

Each deliverable package file will combine data for a single IP.

[vmethod: Analysys]

Requirement IS-IPDE-04 :

Each IP will have its own serial version tag number indicated in package file name and package directory structure.

[vmethod: Analysys]

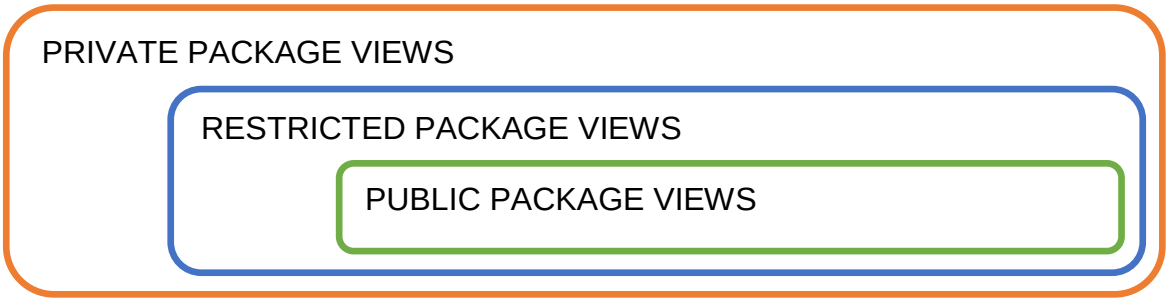
2.1. IP VIEW CLASSIFICATION

Requirement IS-IPDE-05 :

IP views are classified in different distribution categories:

- Public: views distributed without restriction to anyone.
- Restricted: views suitable for distribution to any user under NDA.
- Private: sensitive proprietary data only disclosed to selected partners under special NDA.

Packages variants will be created for every IP to combine views for each distribution scope.



[vmethod: Analysys]

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2.2. IP VIEWS

Requirement IS-IPDE-06 :

The table below indicates a minimum set of recommended IP views that should be distributed in order to support digital and analog design flows. Certain views apply only to selected types of IP blocks, as indicated in the table.

[vmethod: Analysys]

Requirement IS-IPDE-07 :

This list is not exhaustive as additional views may be required for certain IPs.

[vmethod: Analysys]

Requirement IS-IPDE-08 :

IP providers and users should agree on the list of deliverable views for each IP before its release, for instance during requirement specification or IP design review.

[vmethod: Analysys]

View Name	Requirements	Required for digital flow	Required for analog flow	Distribution
Product brief	PDF	Yes	Yes	Public
Release notes	PDF	Yes	Yes	Public
User manual with integration guidelines	PDF	Yes	Yes	Restricted
Black-box OA library • Symbol • Spectre • Eldo • auCdl • auLvs • Abstract	Cadence IC61 compatible	No	Yes	Restricted
Black-box CDL netlist		No	Yes	Restricted
LEF	DEF/LEF version 5.8	Yes	No	Restricted
Encrypted LPE Spectre netlist	Cadence IC61 compatible	No	Yes	Restricted
Encrypted LPE Eldo netlist		No	Yes	Restricted
Liberty file		Yes	No	Restricted
Synopsys compiled DB library		Optional	No	Restricted
Datasheets with Liberty information	PDF or HTML	Optional	Optional	Restricted

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View Name	Requirements	Required for digital flow	Required for analog flow	Distribution
Verilog library models with timing annotation	SDF version 3.0	Yes	No	Restricted
VITAL library models with timing information	SDF version 3.0	Optional	No	Restricted
Verilog-A models (analog IP only)		Yes	Yes	Restricted
IBIS models (digital I/O only)	IBIS version 4.2 or greater	Yes	Yes	Restricted
SPEF file (eFPGA only)		Yes	No	Restricted
GDSII layout		Yes	Yes	Private
CDL netlist		Yes	Yes	Private
LPE Spectre netlist		No	Yes	Private
LPE Eldo netlist		No	Yes	Private
OA library • Symbol • Schematic • Layout	Cadence IC61 compatible	No	Yes	Private

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2.3. PACKAGE STRUCTURE

Requirement IS-IPDE-09 :

All package views will be arranged in a standardized directory structure as shown below. File names and extensions for each view are indicated in this template.

[vmethod: Analysys]

Requirement IS-IPDE-10 :

Additional views not foreseen in this document should be placed in separate subdirectories at the same level as other views, under *Back_End*, *Front_End* or *Documentation* directories, depending on which design phase they are mainly used.

[vmethod: Analysys]

```
PLATFORM_NAME                                   e.g. DARE180XH
`-- IP_NAME                                     e.g. IO
    `-- vVERSION_TAG                            See paragraph 0
        |-- Back_End                            Directory for back-end design views
        |   |-- gds
        |   |   `-- METAL_STACK_NAME            e.g. 1143
        |   |       `-- PLATFORM_IP_NAME.gds.gz e.g. DARE180XH_IO.gds.gz
        |   |-- lef
        |   |   `-- METAL_STACK_NAME
        |   |       `-- PLATFORM_IP_NAME.gds.gz
        |   |-- lpe                             Optional set of PEX corners and parasitic modes
        |   |   |-- spectre
        |   |   |   |-- norc
        |   |   |   |   |-- PLATFORM_IP_NAME.min.scs
        |   |   |   |   |-- PLATFORM_IP_NAME.typ.scs
        |   |   |   |   `-- PLATFORM_IP_NAME.max.scs
        |   |   |   |-- c
        |   |   |   |-- rc
        |   |   |   `-- rcc
        |   |   |-- eldo
        |   |   |   |-- norc
        |   |   |   |   |-- PLATFORM_IP_NAME.min.cir
        |   |   |   |   |-- PLATFORM_IP_NAME.typ.cir
        |   |   |   |   `-- PLATFORM_IP_NAME.max.cir
        |   |   |   |-- c
        |   |   |   |-- rc
        |   |   |   `-- rcc
        |   |-- lpe_encrypt
        |   |   |-- spectre
        |   |   |   |-- norc
        |   |   |   |   |-- PLATFORM_IP_NAME.min.scs
        |   |   |   |   |-- PLATFORM_IP_NAME.typ.scs
        |   |   |   |   `-- PLATFORM_IP_NAME.max.scs
        |   |   |   |-- c
        |   |   |   |-- rc
```

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```
|   |   |   `-- rcc
|   |   |-- eldo
|   |   |   |-- norc
|   |   |   |   |-- PLATFORM_IP_NAME.min.cir
|   |   |   |   |-- PLATFORM_IP_NAME.typ.cir
|   |   |   |   `-- PLATFORM_IP_NAME.max.cir
|   |   |   |-- c
|   |   |   |-- rc
|   |   |   `-- rcc
|   |-- OA
|   |   `-- PLATFORM_IP_NAME
|   |       |-- CELL_NAME_1
|   |       |   |-- abstract
|   |       |   |   `-- layout.oa
|   |       |   |-- auCdl
|   |       |   |   `-- symbol.oa
|   |       |   |-- auLvs
|   |       |   |   `-- symbol.oa
|   |       |   |-- eldo
|   |       |   |   `-- symbol.oa
|   |       |   |-- layout
|   |       |   |   `-- layout.oa
|   |       |   |-- schematic
|   |       |   |   `-- sch.oa
|   |       |   |-- spectre
|   |       |   |   `-- symbol.oa
|   |       |   |-- symbol
|   |       |   |   `-- symbol.oa
|   |       |   `-- data.dm
|   |       |-- ...
|   |       `-- CELL_NAME_n
|   |-- ibis
|   |   `-- platform_ip_name.ibs                Lower case file name required by IBIS standard
|   |-- spef
|   |-- cdl
|   |   `-- PLATFORM_IP_NAME.cdl
|   `-- cdl_bbox
|       |-- PLATFORM_IP_NAME.svrf               SVRF commands for black-box setup
|       `-- PLATFORM_IP_NAME.cdl
|-- Documentation                               Directory for documentation files
|   |-- datasheets
|   |   |-- CORNER_1
|   |   |   `-- index.html
|   |   |-- ...
|   |   `-- CORNER_n
|   `-- documents
|       |-- PLATFORM_IP_NAME_ProductBrief.pdf
|       `-- PLATFORM_IP_NAME_UG.pdf
`-- Front_End                                   Directory for front-end design views
    |-- timing_power_noise
    |   |-- PLATFORM_IP_NAME_CORNER_1.lib
    |   |-- ...
```

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```
|   `-- PLATFORM_IP_NAME_CORNER_n.lib
|-- veriloga
|   `-- PLATFORM_IP_NAME.va
|-- verilog
|   `-- PLATFORM_IP_NAME_SDF3_0.v
`-- vital
    `-- PLATFORM_IP_NAME_SDF3_0.vhd
```

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2.4. VERSION TAGGING

Requirement IS-IPDE-11 :

IP version tagging intends to enable full traceability of data and versions used in designs.

[vmethod: Analysys]

Requirement IS-IPDE-12 :

IP version numbers should comply to the format V*x_y_z*, where *x* integer indicates a major update, *y* integer indicates a minor update, and *z* indicates a version number relevant internally to the IP provider. Example: DARE180XH_CORE_V2.1.349.

[vmethod: Analysys]

Requirement IS-IPDE-13 :

Version numbers must be included in the package name and its directory structure, as shown in paragraph2.3.

[vmethod: Analysys]

Requirement IS-IPDE-14 :

IP version and ownership information should be placed in all documentation, GDSII and text-format views. In the case of text files, header comments can be used, as shown in the example below. IP providers are free to use their own formatting style.

[vmethod: Analysys]

DARE180XH_PLL.lef:

```
#*****************************************************************************
#* DARE180XH Platform                                                        *
#* Copyright 2020, imec vzw. All Rights Reserved.                            *
#* Technical support: dare_support@imec.be                                   *
#*---------------------------------------------------------------------------*
#* Library : DARE180XH_PLL                                                   *
#*                                                                           *
#* Release version : 1.0.321                                                 *
#* Release date    : 22-Apr-2020 23:31                                       *
#*****************************************************************************

VERSION 5.8 ;
...
```

Requirement IS-IPDE-15 :

In the case of GDSII, tags should be added and encoded in accordance with the VSIA's IP tagging standard (RD1).

[vmethod: Analysys]

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3. DELIVERABLE DATA VALIDATION [DDVA]

Requirement IS-DDVA-16 :

IP views must be validated upon release to users by its design house. Certain sanity checks will also be performed at imec upon starting top-level designs using deliverables from IP providers.

[vmethod: Analysys]

Requirement IS-DDVA-17 :

A minimum required set of verification procedures is defined in this section.

[vmethod: Analysys]

3.1. SINGLE VIEW CHECKS

Requirement IS-DDVA-18 :

Several verification procedures must be applied on individual IP views.

[vmethod: Analysys]

Check	Views	Method (Tool)	Responsible
Foundry design rules (DRC)	Layout GDSII OA abstract	Automated (Calibre/PVS)	IP designer + imec
Foundry antenna rules	Layout GDSII	Automated (Calibre/PVS)	IP designer + imec
DARE layout rules (RAD)	Layout GDSII	Automated (Calibre)	IP designer
Routability of block terminals (pin placement, access...)	Layout GDSII OA abstract LEF	Automated (script)	IP designer + imec
Library cell template and abutment	Layout GDSII OA abstract LEF	Automated (script)	imec
Mask layer numbers	GDSII	Automated (script)	IP designer + imec
Library/IP cell list completeness	*all*	Automated (script)	IP designer + imec
Characterization data value consistency	Liberty	Automated (Library Compiler)	IP designer

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Check	Views	Method (Tool)	Responsible
Liberty file syntax and semantics	Liberty	Automated (Library Compiler)	IP designer + imec
HDL file syntax	Verilog VITAL	Automated (Modelsim)	IP designer + imec
IBIS syntax	IBIS	Automated (ibis_chk)	imec

3.2. CROSS-VIEW CHECKS

Requirement IS-DDVA-19 :

Design tools require matching information across different views. Several consistency checks between views must be performed by IP providers and imec top-level designers.

[vmethod: Analysys]

Check	Cross Views	Method (Tool)	Responsible
All views present	all	Automated (script)	IP designer + imec
All cells present	all	Automated (script)	IP designer + imec
Matching pin order	CDL vs. OA symbol CDL vs. PEX netlist CDL vs. PEX netlist CDL vs. encrypted PEX netlist CDL vs. black-box CDL CDL vs. Verilog CDL vs. Verilog-A	Automated (script)	IP designer
Matching pin name, type and direction	all	Automated (script)	IP designer + imec
Layout versus Schematic (LVS)	GDSII vs. CDL OA abstract vs. black-box CDL	Automated (Calibre/PVS)	IP designer + imec
Matching SDF annotation	Liberty vs. Verilog	Automated (Liberate)	IP designer + imec

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4. DESIGN FLOWS [DFLW]

Requirement IS-DFLW-20 :

This section describes the use of distributed IP views in analog-on-top and digital-on-top methodologies for ASIC design. As well, the digital-on-top flow can be used to implement digital circuits for complex mixed-signal IP blocks which are designed using the analog-on-top methodology.

[vmethod: Analysys]

4.1. ANALOG-ON-TOP FLOW

Requirement IS-DFLW-21 :

Analog-on-top methodology employs a schematic-driven flow to implement analog-centric designs with small amounts of digital logic. In this flow, designers must place all blocks in the design and route all signals by hand.

This flow is preferred for analog and mixed-signal IP design. As well, it may be used for top-level chip design mainly in the case of purely analog systems.

Tools for analog-on-top design include design tools (e.g. Cadence Virtuoso), physical verification tools (e.g. Cadence PVS) and functional verification tools (e.g. Cadence Spectre).

Analog-on-top design may require the following views:

- OA symbol/spectre/auCdl/auLVS
- GDSII or OA layout or black-box OA abstract
- CDL netlist or OA schematic or black-box CDL netlist
- PEX netlist or encrypted PEX netlist

[vmethod: Analysys]

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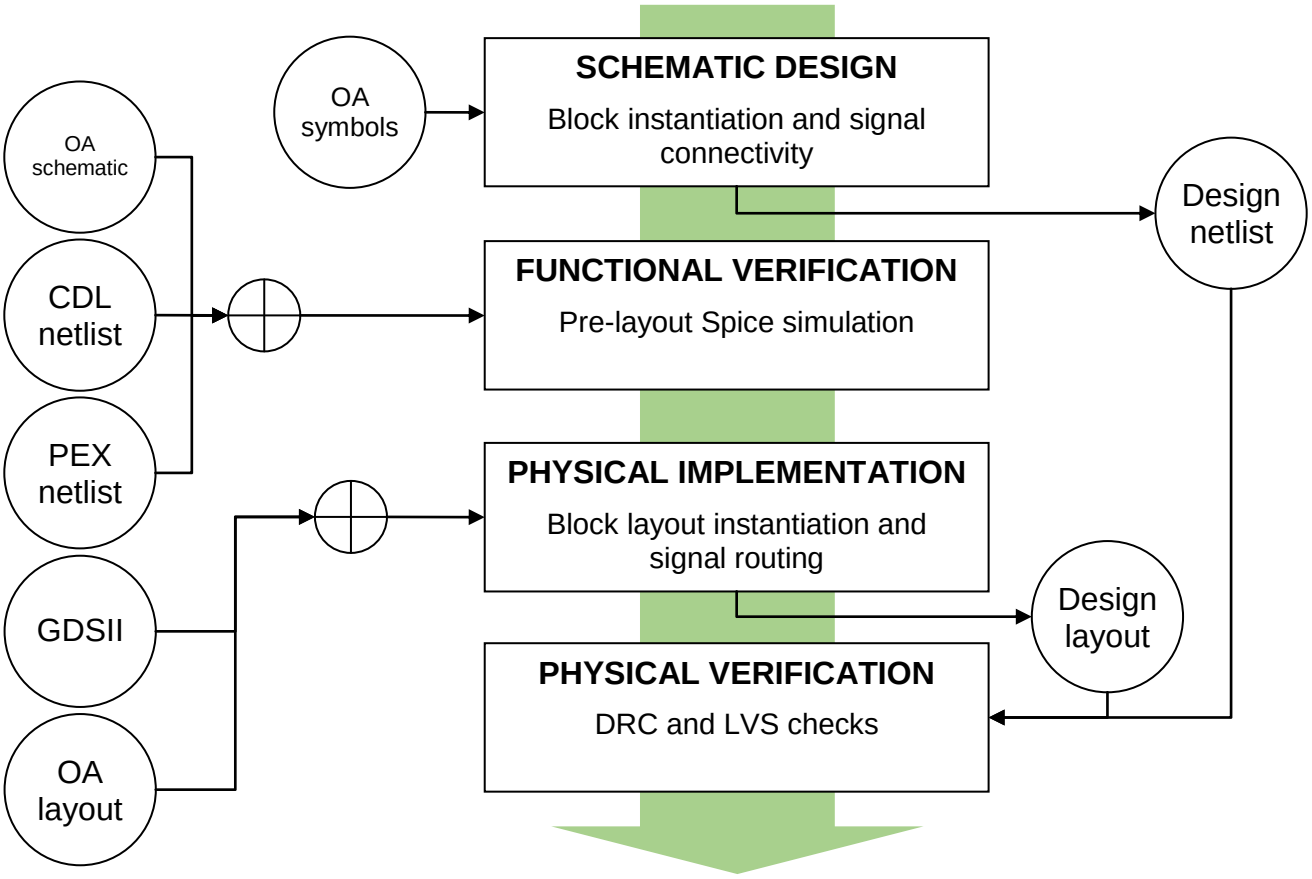
4.1.1. Analog Design Flow Using Full Design Views

A typical analog design flow using full design views is depicted in the diagram below.



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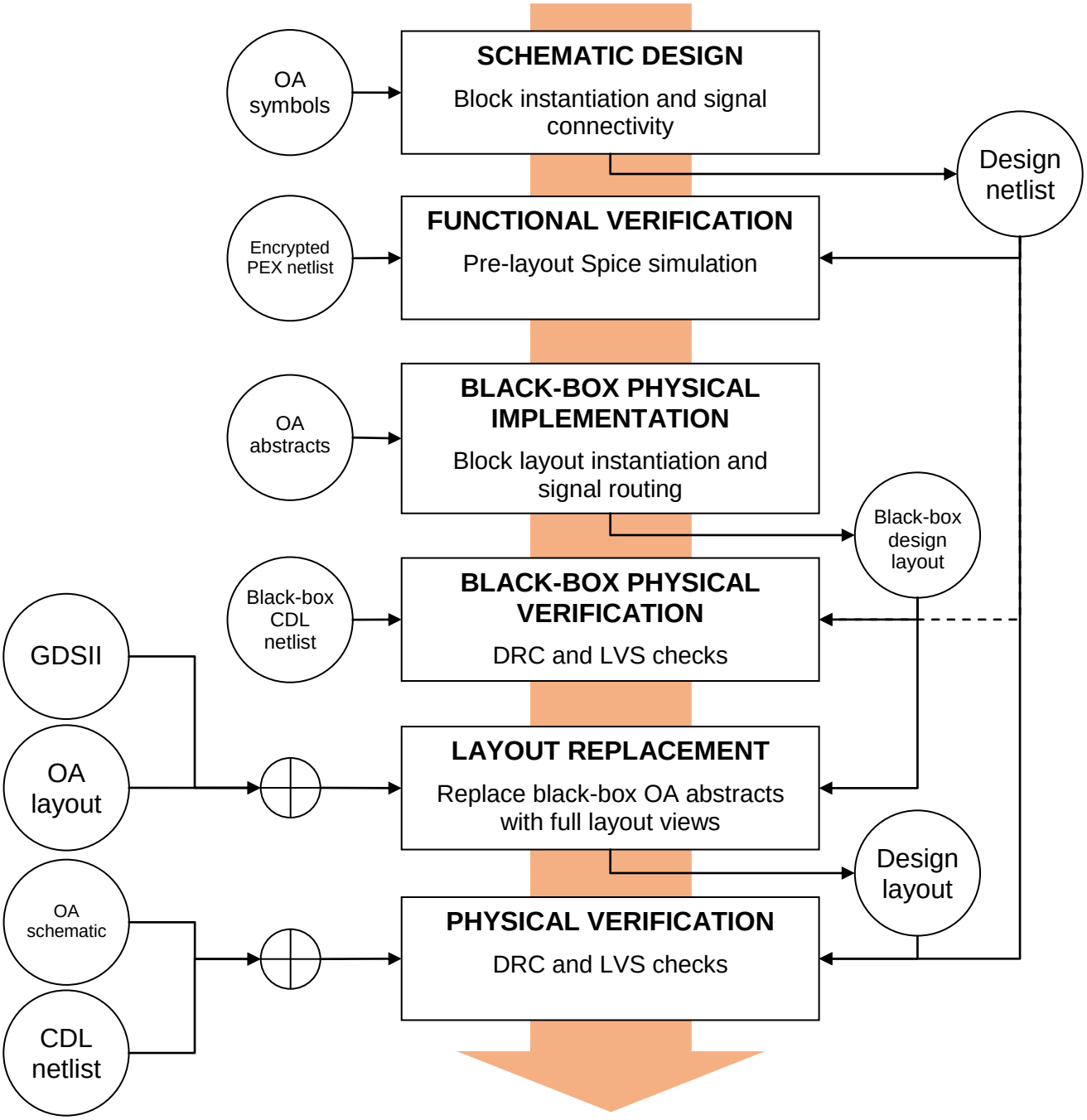
4.1.2. Analog Design Flow Using Black-Box Design Views

In case GDSII/OA layout and CDL/OA schematic views are not available, it is possible to implement designs using black-box views. In this case, additional actions are required to obtain final tape-out layout by replacing black-box views with full views, as depicted in the diagram below.



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4.2. DIGITAL-ON-TOP FLOW

Requirement IS-DFLW-22 :

Digital-on-top methodology uses a high-level netlist-driven flow to implement designs with large amounts of digital logic. In such flow, high levels abstraction and tool automation are employed to handle complex design and verification tasks which require additional library views.

Tools for digital-on-top design include functional verification tools (e.g. Mentor Modelsim), physical design tools (e.g. Cadence Innovus) and physical verification tools (e.g. Cadence PVS).

Digital-on-top design requires at least the following views:

- GDSII
- LEF
- CDL netlist
- Liberty file or Synopsys DB library
- Verilog or VITAL library models

In addition, digital flows require design views such as functional high-level RTL design description (Verilog or VITAL) and constraint specification (SDC).

[vmethod: Analysys]

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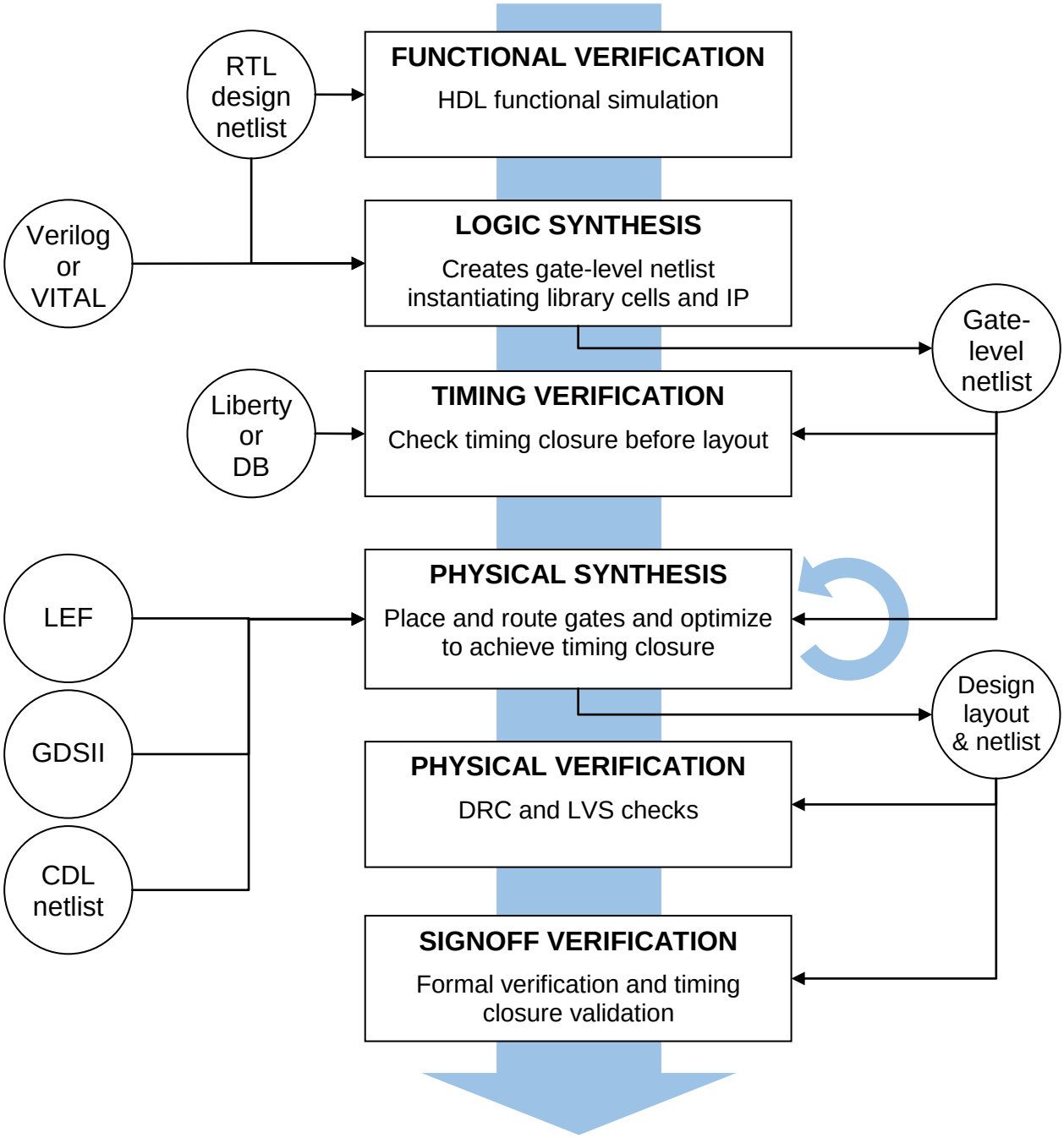
A basic digital-on-top flow is depicted in the diagram below.



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4.3. MIXED-SIGNAL DESIGN

Requirement IS-DFLW-23 :

Analog and digital flows can be combined in the design of complex mixed-signal applications.

Although analog-on-top methodology is mainly used to design IP blocks for later use in digital-on-top flows, designers implementing complex IPs with large digital functions (e.g ADC) can also make use of the digital flows to design digital parts of such blocks in an automated way. Digital-on-top outputs (e.g GDSII, CDL netlist) can then be imported in analog-on-top flows to be combined with other circuit components.

[vmethod: Analysys]

5. COMPLIANCE MATRIX

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Reference	Description	Compliance	Verification method
IS-IPDE-01	IP deliverables refer to the set of library or IP views provided by any partner design house.		
IS-IPDE-02	IPdeliverabledatawillbedistributedintarballcompressedpackagefilescontainingviews anddocumentationarrangedinapredefineddirectorystructure.		
IS-IPDE-03	Each deliverable package file will combine data for a single IP.		
IS-IPDE-04	Each IP will have its own serial version tag number indicated in package file name and package directory structure.		
IS-IPDE-05	IP views are classified in different distribution categories: Public: views distributed without restriction to anyone. Restricted: views suitable for distribution to any user under NDA. Private: sensitive proprietary data only disclosed to selected partners under special NDA. Packages variants will be created for every IP to combine views for each distribution scope.		
IS-IPDE-06	The table below indicates a minimum recommended IP views that should be distributed in order to support digital and analog design flows. Certain views apply only to selected types of IP blocks, as indicated in the table.		
IS-IPDE-07	ThislistisnotexhaustiveasadditionalviewsmayberequiredforcertainIPs.		
IS-IPDE-09	All package views will be arranged in a standardized directory structure as shown below. File names and extensions for each view are indicated in this template.		
IS-IPDE-10	Additional views not foreseen in this document should be placed in separate subdirectories at the same level as other views, under Back_End, Front_End or		

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Reference	Description	Compliance	Verification method
	Documentation directories, depending on which design phase they are mainly used.		
IS-IPDE-11	IP version tagg intends to enable full traceability of data and versions used in designs.		
IS-IPDE-12	IP version numbers should comply to the format Vx_y_z, where x integer indicates a major update, y integer indicates a minor update, and z indicates a version number relevant internally to the IP provider. Example: DARE180XH_CORE_V2.1.349.		
IS-IPDE-13	Versionnumbersmustbeincludedinthepackagenameanditsdirectorystructure,asshowninparagraph2.3.		
IS-IPDE-14	IP version and ownership information should be placed in all documentation, GDSII and text-format views. In the case of text files, header comments can be used, as shown in the example below. IP providers are free to use their own formatting style.		
IS-IPDE-15	In the case of GDSII, tags should be added and encoded in accordance with the VSIA's IP tagging standard (RD1).		
IS-DDVA-16	IP views must be validated upon release to users by its design house. Certain sanity checks will also be performed at imec upon starting top-level designs using deliverables from IP providers.		
IS-DDVA-17	A minimum required set of verification procedures is defined in this section.		
IS-DDVA-18	Several verification procedures must be applied on individual IP views.		
IS-DDVA-19	Design tools require matching information across different views. Several consistency checks between views must be performed by IP providers and imec top-level designers.		
IS-DFLW-20	This section describes the use of distributed IP views in analog-on-top and digital-		

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Reference	Description	Compliance	Verification method
	on-top methodologies for ASIC design. As well, the digital-on-top flow can be used to implement digital circuits for complex mixed-signal IP blocks which are designed using the analog-on-top methodology.		
IS-DFLW-21	Analog-on-top methodology employs a schematic-driven flow to implement analog-centric designs with small amounts of digital logic. In this flow, designers must place all blocks in the design and route all signals by hand. This flow is preferred for analog and mixed-signal IP design. As well, it may be used for top-level chip design mainly in the case of purely analog systems. Tools for analog-on-top design include design tools (e.g. Cadence Virtuoso), physical verification tools (e.g. Cadence PVS) and functional verification tools (e.g. Cadence Spectre). Analog-on-top design may require the following views: OA symbol/spectre/auCdl/auLVS GDSII or OA layout or black-box OA abstract CDL netlist or OA schematic or black-box CDL netlist PEX netlist or encrypted PEX netlist		
IS-DFLW-22	Digital-on-top methodology uses a high-level netlist-driven flow to implement designs with large amounts of digital logic. In such flow, high levels abstraction and tool automation are employed to handle complex design and verification tasks which require additional library views. Tools for digital-on-top design include functional verification tools (e.g. Mentor Modelsim), physical design tools (e.g. Cadence Innovus) and physical verification tools (e.g. Cadence PVS). Digital-on-top design requires at least the following views:		

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Reference	Description	Compliance	Verification method
	GDSII LEF CDL netlist Liberty file or Synopsys DB library Verilog or VITAL library models In addition, digital flows require design views such as functional high-level RTL design description (Verilog or VITAL) and constraint specification (SDC).		
IS-DFLW-23	Analog and digital flows can be combined in the design of complex mixed-signal applications. Although analog-on-top methodology is mainly used to design IP blocks for later use in digital-on-top flows, designers implementing complex IPs with large digital functions (e.g ADC) can also make use of the digital flows to design digital parts of such blocks in an automated way. Digital-on-top outputs (e.g GDSII, CDL netlist) can then be imported in analog-on-top flows to be combined with other circuit components.		

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