PROMISE

WP3 Supply Chain Definition
D3.2 Qualification Plan Standard

Written by	***Responsibility*** + handwritten signature if no electronic workflow tool
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CHANGE RECORDS

ISSUE	DATE	§ CHANGE RECORDS	AUTHOR
001	06/03/2020	Initial Version	M. Carquet
002	19/04/2020	Final version after reviews for submission	M. Carquet and F. Veljković

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1. PURPOSE

It is here after reminded the purpose of Task 3.2 of Work Package Number WP3 “Supply Chain Definition”, as described in the Grant Agreement Number 870358 – PROMISE – H2020-SPACE-2018-2020 / H2020-SPACE-2019.

Task 3.2: Define Qualification Plan Standard (M1-M3) - Leader: TASF - Participants: TASE, VTT
In this task, TASF with the support of TASE shall define the Qualification Plan Standard. This plan shall include a detailed description of all the tests to be performed for silicon qualification (radiation, HTOL, ESD, NVM retention and endurance, etc…). The environmental and mechanical tests are specific to package and are out of the scope of circuit qualification at silicon level.
The Qualification plan Standard shall clearly define how embedded IPs and a circuit top level are covered; it will help future end-user to decide what can be the savings of re-use already silicon qualified IPs.
The Qualification Plan Standard documentation shall be issued as task output and the review corresponding to milestones shall be held.
The related documentation shall be provided to TASF for future use by End-user.
In order to reach the targeted TRL the consortium will follow ESCC 9000 as per attached diagram. The following test campaign is foreseen for the PROMISE Pilot Circuit:
• Electrical tests at hot, ambient and cold temperature
• Radiation tests
• Life Tests including electrical tests
• LAT of the packaged device is foreseen but it extend and details will depend on the final package and packaging company selected. As baseline ESCC 9000 will be followed. ESCC 9000 standard includes two families of tests:
o Die related tests: These include electrical performance tests, electrical life tests, thermal tests, radiation tests, etc…
o Package related tests: These include hermeticity, vibration, bond pulling, marking, etc…
Once the final packaging for the Pilot Circuit is selected based on cost and performance criteria, the heritage of that packaging will be reviewed. According to ESA rules, the package related tests can be spared if there are previous data available (not older than 2 years) for an specific test that is related to the packaging manufacturing and has no relation with the die performance (e.g.: Hermeticity test is related with the sealing process of the package and is independent of the die that is inside the package cavity).

This proposed sequence shall be completed on both runs of the device. However, the full execution on run 1 will depend of the findings that the different tests reveal.
The tests shall characterize the entire Pilot Circuit as well as each of the independent IPs. Full details of the different tests to be executed shall be agreed by the partners and included in D5.1, D5.2 and D5.3.
This campaign will be executed on the PROMISE Pilot Circuit and shall validate both the circuit and its constituent IPs.

Per this purpose, the present document is the Deliverable Number D3.2 “Qualification Plan Standard”.

It will be used as input for the WP3 Task 3.3: Identify European actors space Mixed-signal ASIC supply chain.

Thales Alenia Space has the end-user role in the PROMISE consortium. Accordingly, during the PROMISE project, Thales Alenia Space will use this Qualification Plan to issue a Procurement Specification dedicated to the PROMISE PILOT Circuit. The PILOT Circuit is handling the qualification at silicon level for the PILOT Circuit itself and for each embedded IP.

This Qualification Plan standard may help an end-user in issuing a Procurement Specification dedicated to its circuit designed using PROMISE library and ecosystem.

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2. RELATED DOCUMENTS

2.1. APPLICABLE DOCUMENTS

When no issue is mentioned, the relevant issue shall be those in effect on the date of starting the components manufacturing or of placing the Purchase Order.

Internal code / DRL	Reference	Issue	Title	Location of record
AD1	ESCC Basic Specification No. 2269000 – ESA document		Evaluation Test Programme for Integrated Circuits : Monolithic and Multichip Microcircuits, Wire-Bonded, Hermetically Sealed and Flip-Chip Monolithic Microcircuits, Solder Ball Bonded, Hermetically and Non-Hermetically Sealed	
AD2	ESCC Generic Specification No 9000 – ESA document		Integrated Circuits : Monolithic and Multichip Microcircuits, Wire-Bonded, Hermetically Sealed and Flip-Chip Monolithic Microcircuits, Solder Ball Bonded, Hermetically and Non-Hermetically Sealed and Die	
AD3	ESCC Basic Specification No 20500 – ESA document		External Visual Inspection	
AD4	ESCC Basic Specification No 21300 – ESA document		Terms, Definitions, Abbreviations, Symbols and Units	
AD5	ESCC Basic Specification No 22900 – ESA document		Total Dose Steady State Irradiation Test Method	
AD6	ESCC Basic Specification No 25100 – ESA document		Single Event Effects Test Method and Guidelines	

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Internal code / DRL	Reference	Issue	Title	Location of record
AD7	MIL-STD-883		Test Method Standard Microcircuits	
AD8	ESDA/JEDEC Joint Standard ANSI/ESDA/JEDEC JS-001-2017		For Electrostatic Discharge Sensitivity Testing - Human Body Model (HBM) – Component Level	
AD9	ESDA/JEDEC Joint Standard ANSI/ESDA/JEDEC JS-002-2014		For Electrostatic Discharge Sensitivity Testing - Charged Device Model (CDM) – Device Level	

2.2. REFERENCE DOCUMENTS

When no issue is mentioned, the relevant issue shall be those in effect on the date of starting the components manufacturing or of placing the Purchase Order.

Internal code / DRL	Reference	Title	Location of record
RD1	870358	Grant Agreement Number 870358 – PROMISE – H2020-SPACE-2018-2020 / H2020-SPACE-2019	
RD2	PROMISE D1.1	Standard for Mixed-Signal IP Cores Design	
RD3	PROMISE D1.3	Interface Standards and IP Usage Definition	
RD4	Document release 03.18 – X-FAB document	0.18µm Process Family XH018 data sheet	Restricted access

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3. ACRONYMS AND ABBREVIATIONS

ADC	Analog-to-Digital Converter
ASIC	Application Specific Integrated Circuit
BIST	Built-In Self Test
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
COTS	Commercial Off The Shelf
CSI	Customer Source Inspection
DAC	Digital-to-Analog Converter
DFT	Design For Testability
DUT	Device Under Test
eFPGA	Embedded Field Programmable Gate Array
ESCC	European Space Components Coordination
ESD	ElectroStatic Discharge
FPGA	Field Programmable Gate Array
HBM	Human Body Model
HTOL	High Temperature Operating Life
IC	Integrated Circuit
IP	Intellectual Property
ITP	Irradiation Test Plan
LDO	Low Drop Out
LO	Local Oscillator
HV MOS	High Voltage Metal Oxide Semiconductor
MBU	Multiple Bit Upset
MCU	Multiple Cell Upset
NVM	Non Volatile Memory
PID	Process Identification Document
PLL	Phase Lock Loop
POR	Power-On Reset
SEE	Single Event Effect
SEFI	Single Event Functional Interrupt
SEL	Single Event Latchup
SET	Single Event Transient
TBC	To Be Confirmed
TBD	To Be Defined
TID	Total Ionising Dose
WP	Work Package

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4. PROMISE CIRCUIT DESCRIPTION

A PROMISE circuit will embed IPs designed during the PROMISE project, and IPs designed after the PROMISE project using the PROMISE ecosystem.

PROMISE designs use the XFab XH018 technology (CMOS 180nm).

A list of these IPs is given herebelow.

eFPGA	~20 x 20 matrix, including DSP columns
ADC	Sigma Delta, Low Sampling Rate, 24 bits max, differential input
DAC	Sigma Delta, 24 bits max, differential current output
PLL	Output Frequency programmable up to 200MHz
LDO	1.8V Output Voltage from 3.3V Input Voltage
BANDGAP	1.25V ±0.2% and 10ppm/°C after tuning
LO	16MHz Output Clock, 50% Duty Cycle
POR	Power-On Reset on AVDD 3.3V and DVDD 1.8V
NVM	50 Blocks of 512 x 32 bits, Read Cycle Time 10 to 40ns (TBC), 4MHz Clock (TBC)
HV MOS	High Voltage N and P MOS transistors

Table 1 – PROMISE IPs List

Details for each IP are available through the PROMISE project website and public access data repositories.
During the PROMISE project, the PILOT Circuit is designed to support and validate the design flow, the manufacturing flow and the qualification flow. The PILOT Circuit, as an example of ASIC designed using PROMISE, embeds all the IPs designed during the project.

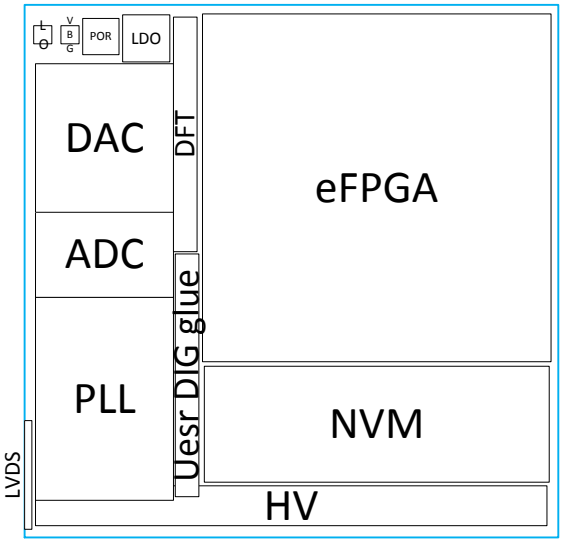

Figure 1 - PILOT Circuit example

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5. PROMISE PILOT CIRCUIT QUALIFICATION PLAN

5.1. GENERAL

A PROMISE Pilot Circuit is designed so that every IP is independently accessible for test.

In the Qualification Plan, some activities will cover the PROMISE Circuit as a global entity (circuit Top level), and other activities will be devoted to cover only a specific IP.

The Supplier is entirely responsible for the respect of the requirements of this Qualification Plan, the activities being either performed in-house or subcontracted.

All results shall be recorded, and failed components submitted to a failure analysis. Probable failure modes and mechanisms shall be determined.

Progress of the components shall be observed closely. A chart showing the numbers in/out and failure cause for each fabrication stage shall be prepared.

5.2. COMPONENTS PRODUCTION AND CONTROL

The tested components shall be issued from a unique and homogeneous lot (diffusion lot and assembly lot – see [AD4] for definitions).

The PILOT Circuit will be hermetically sealed and will have a ceramic body.

The components shall not have been submitted to any screening or burn-in, but must have been manufactured in conformity with high reliability practice and an established Process Identification Document (PID) or an identifiable process which shall form the basis for the PID.

Internal visual inspections shall be performed on the lot to be tested to the extent that this forms part of the Supplier's standard procedures.

The end-user shall prepare a Detail Specification in accordance with the established ESCC format.

This shall then serve as a basis for the testing of the components.

5.3. INSPECTION

The components shall be checked to verify their suitability for the Qualification test programme. For each measurement or inspection performed, the results shall be summarised in terms of quantity tested, quantity passed and quantity rejected. If devices are rejected, the reason shall be clearly identified.

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5.3.1. External visual inspection (100%)

All devices shall be inspected (Go/No Go) in accordance with :

[AD3]

Rejected components shall be replaced.

5.3.2. Particle Impact Noise Detection (PIND)(100%)

All devices shall be tested in accordance with conditions defined in [AD2], i.e. :

[AD7], Test Method 2020, Test Condition A.

Rejected components shall be replaced.

5.3.3. Radiography (100%)

All devices shall be tested in accordance with conditions defined in [AD1], i.e. :

[AD7], Test Method 2012.

Rejected components shall be replaced.

5.3.4. Hermeticity (100%)

All devices shall be submitted to fine and gross leak tests in accordance with conditions defined in [AD2], i.e. :

Fine leak : [AD7], Test Method 1014, Condition A or B

Gross leak : [AD7], Test Method 1014, Condition C

Rejected components shall be replaced.

5.3.5. Marking and Serialisation (100%)

All components shall be marked and serialised, so that traceability and data recording is ensured throughout all the test activities.

5.3.6. Completion of inspection

The completion of inspection shall result in a batch of components that have been verified as to their suitability for the Qualification Test Programme, i.e. each component has satisfied the requirements of paragraphs 5.3.1 to 5.3.5 inclusive.

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5.3.7. Initial Electrical Measurements (100%)

5.3.7.1. TEST PROGRAMME DEFINITION

The PROMISE circuits are embedding Design For Testability (DFT) capabilities described in [RD2] and [RD3].

More details will be added when [RD2] are [RD3] are more mature.

5.3.7.2. ELECTRICAL TESTS

These measurements shall be made according to the Room, High and Low Temperatures electrical measurement conditions and limits listed in the Detail Specification.

All measurements results shall be recorded against serial numbers.

5.4. QUALIFICATION TEST PROGRAMME

The test program for silicon qualification is presented in Figure 2 hereafter.

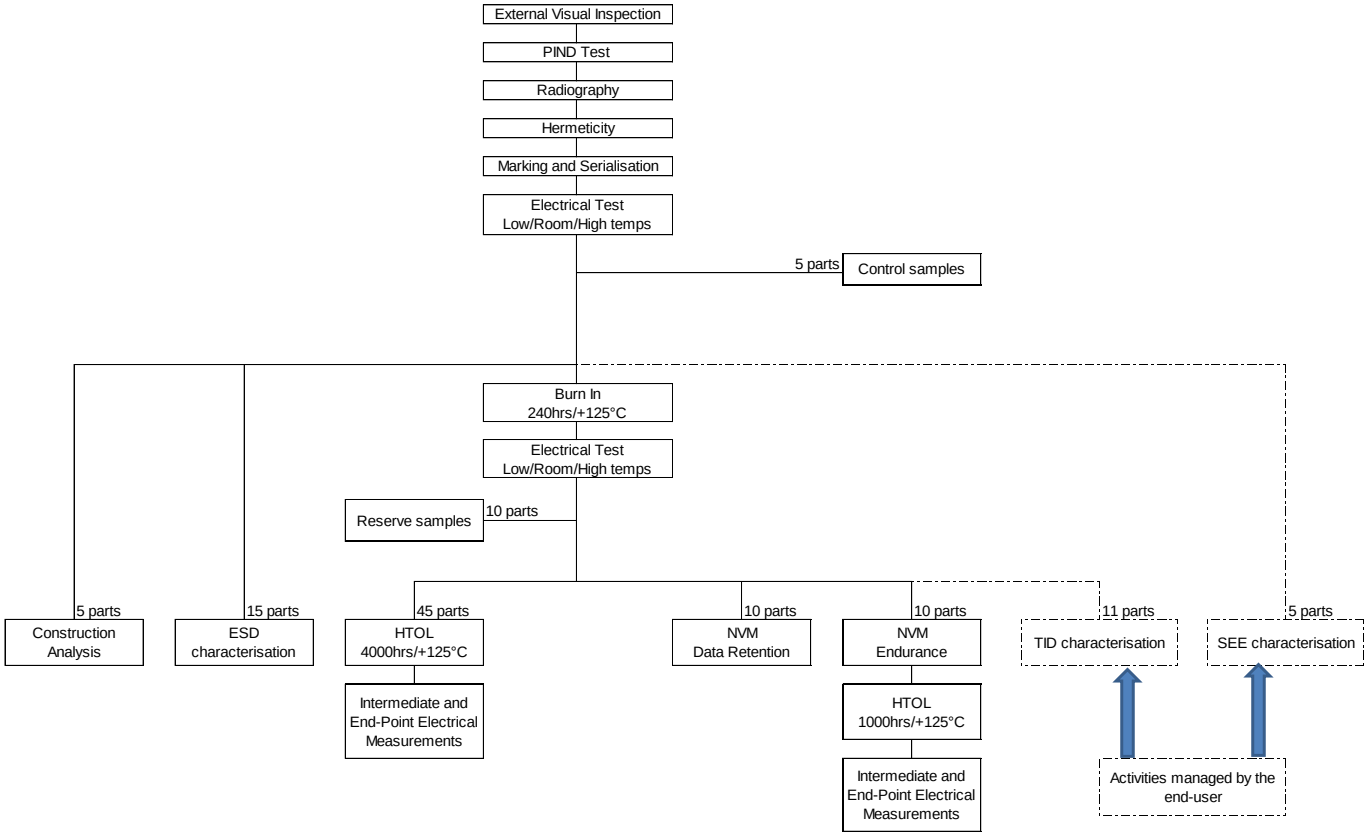

Figure 2 - Silicon Qualification Test Programme

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Deviations to these test requirements may be approved subject to full justification being provided.

Approved deviations shall be fully documented and all details shall be included in the Qualification report.

5.4.1. General

The components shall be randomly divided into groups in the quantities indicated in Figure 2.

All failed components shall be analysed. The depth of analysis shall depend upon the circumstances in which failure occurred and upon useful information may be gained. As a minimum, the failure mode shall be determined in each case. Components not failing catastrophically, i.e. those displaying out-of-tolerance electrical parameters, shall not be removed from the test sequence but monitored to observe degradation trends.

5.4.2. Control samples

These components shall be retained for comparison purpose.
Whenever electrical measurements are made on any device under test, these devices shall also be measured (“golden samples”).

5.4.3. Reserve samples

These components shall be retained for the following purpose :
- use for any additional tests be considered necessary,
- replacement of any damaged or lost part.

5.4.4. Construction Analysis

A Construction Analysis shall be performed to detect any design or construction defect which may affect the reliability of the components and to facilitate failure analysis activities.

The Construction Analysis shall be performed using [AD1] as a guideline.

Items related to packaging should be omitted.

5.4.5. ESD Characterisation

An ESD characterisation shall be performed in accordance with the following requirements.

- for Human Body Model (HBM) :

[AD7], Test Method 3015

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[AD8] may be used as an alternate method.

- for Charged Device Model (CDM) :

[AD9]

5.4.6. Burn-In

Some tests require that the parts are submitted to a Burn-In equivalent to those seen by Flight Models prior to testing.

Burn-In shall be performed in accordance with the requirements of [AD2], i.e. :

[AD7], Test Method 1015

Duration : unless otherwise specified in the Detail Specification, Burn-in duration shall be 240 (+24 -0) hours.

Test Condition : as specified in the Detail Specification.

Data points :
as specified in Parameter Drift Values in the Detail Specification. Drift shall be related to the initial measurement for Burn-In.
These measurements shall be made according to the Room, High and Low Temperatures electrical measurement conditions and limits listed in the Detail Specification.
All measurements results shall be recorded against serial numbers.

5.4.7. High Temperature Operating Life

High Temperature Operating Life (HTOL) with the requirements of [AD2], i.e. :

[AD7], Test Method 1005

Duration : HTOL duration shall be 4000 hours.

Test Conditions : as specified in the Detail Specification.

Data points :
as specified in in Intermediate and End-Point Parameter Electrical Measurements in the Detail Specification at 0 hour, 1000 ±48 hours, 2000 ±48 hours, 3000 ±48 hours and 4000 ±48 hours.
These measurements shall be made according to the Room, High and Low Temperatures electrical measurement conditions and limits listed in the Detail Specification.
All measurements results shall be recorded against serial numbers.

If drift values are specified, the drift shall always be related to the 0 hour measurement.

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5.4.8. NVM Data Retention

A Data Retention test shall be performed for initial characterisation.

The method and procedure will be adapted to the type of NVM implemented.

To be able to cover any Space mission profile, they shall guarantee a 20 years Data Retention time over the -55°C/+125°C temperature range.

5.4.9. NVM Endurance

A reprogrammability test shall be performed for initial characterization.

The method and procedure will be adapted to the type of NVM implemented.

They shall guarantee 10,000 (TBC) Program/Erase cycles over the -55°C/+125°C temperature range.

A 1000 hours/+125°C HTOL, with readouts at 168/500/1000 hours, shall be performed after the 10,000 Program/Erase cycles, to demonstrate that the reliability in not impaired by the programming cycles.

5.4.10. Total Ionising Dose (TID) test

This activity will be managed by the end-user.

The Supplier shall provide the end-user with the parts quantity indicated in Figure 2 plus at least 1 control sample.

Components will be characterised using “low rate” window as defined in [AD5] : between 36 rad(Si)/h and 360 rad(Si)/h.

The following figure shows the global TID test procedure : 12 samples shall be available and functionally tested. To validate the complete lot, the number of samples defined in [AD5] will be necessary.

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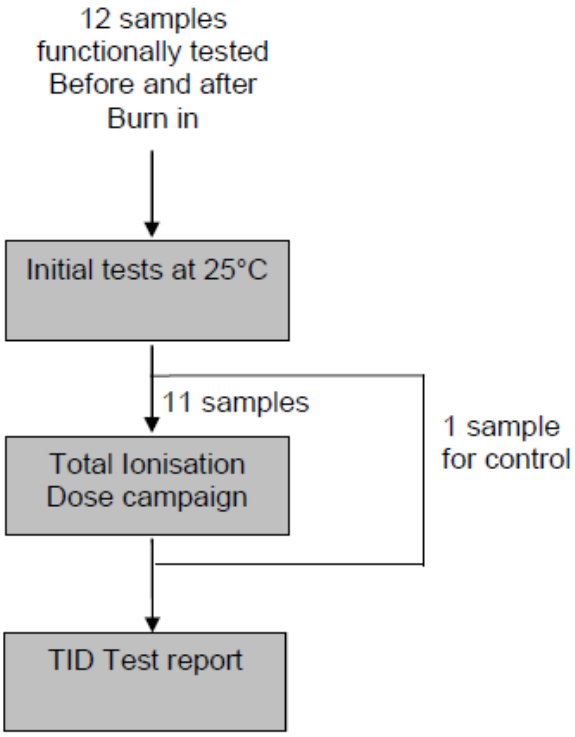

Figure 3 - TID test procedure

The samples are tested before the ionization campaign to get the initial characteristics for the TID drift calculation.

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5.4.10.1. TID TESTS CAMPAIGN

The TID tests campaign is then run up to 100 krads, with steps at roughly 10, 20, 50 and 100 krads and followed by annealing and final electrical tests to detect eventual parameter bounce :

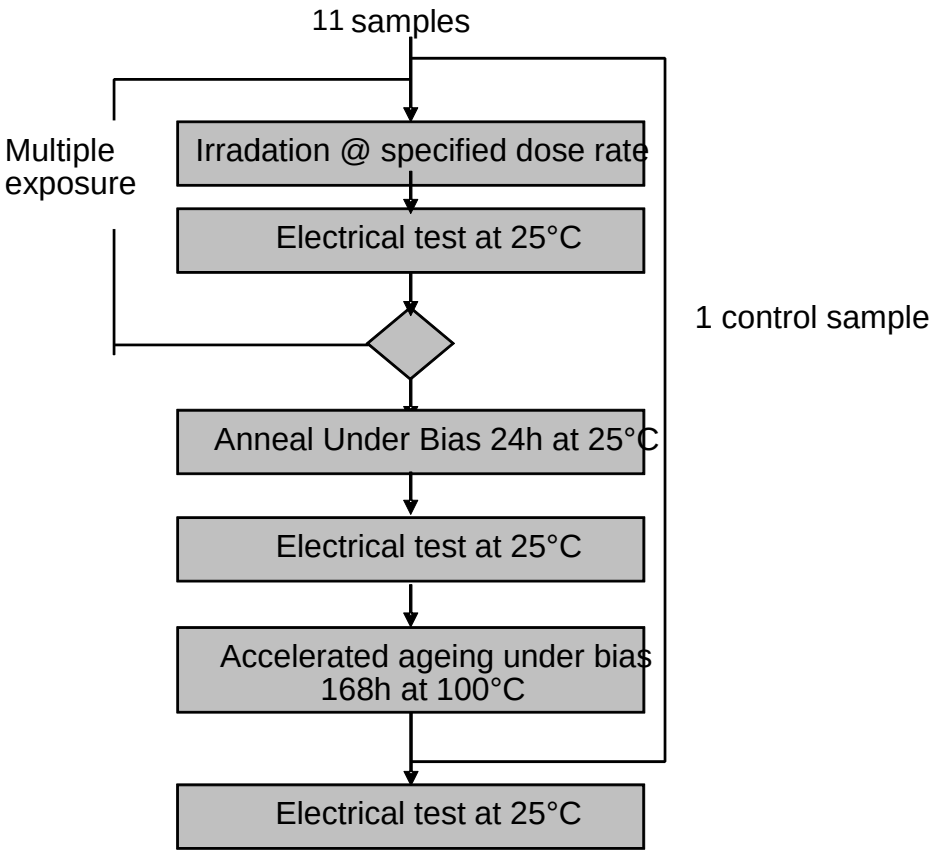

Figure 4 - TID test campaign description

At the beginning of the campaign, at each dose step, and at each annealing step, the electrical test results are logged and the drift of each parameter versus initial test is calculated.
At each of these steps, the non-irradiated control sample shall be measured as well.
The TID test procedure and configuration, the TID campaign description and all the results will be reported in a specific document. A dedicated Irradiation Test Plan (ITP) shall be issued.

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5.4.10.2. TID REQUIRED HARDWARE

The required hardware is based on the usual approach for TID test, based on the electrical validation system developed.

Exposure board
Dedicated boards will be manufactured for TID exposure providing the different biasing (Power-On and sequenced, power-shut-down for example). The exposure board design and construction shall be consistent with high temperature to support the accelerated ageing step. At prototype level, this board can be used also for the initial burn-in before initial test ; in that case, it shall support +125°C.

Test board
Dedicated boards will be manufactured to allow the electrical tests at room temperature; the test list shall be according the different embedded IPs.

Sockets
Sockets (TBC) for the TID boards may be required :
- 12 for the biasing board (irradiation exposure)
- 4 for the test board

The socket design and construction shall be consistent with the +100°C temperature, respectively +125°C if used for burnin.

5.4.10.3. CONFIGURATION AND BIAS UNDER TID EXPOSURE

The components shall be configured and biased according the following values :
- 5 samples are supplied and dynamically sequenced by clocks at freq. max (kHz).
- 3 samples are supplied and in powershutdown mode (if available) or not sequenced by clocks (static).
- 3 samples are grounded.

The control sample is not irradiated.

5.4.10.4. ELECTRICAL TEST BENCH

The electrical tests performed on the devices during TID campaign at each step will be detailed in the dedicated ITP.
Test automation strategy and eventually the number of tests (on noise and linearity) shall be adapted to allow the test of all the samples during the time available between 2 irradiation steps.

5.4.10.5. FUNCTIONAL AND PERFORMANCES TESTS

The Tests shall cover as much as possible the functionalities and performances described in each IP including:
- Supply Operating Current: (VCCxx)

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- Reference voltage:
- Reference current
- Digital IO performances (VIH, VOL, ...)

The objective is to define the main electrical parameters and evaluate their degradation that may cause a noticeable degradation of performance at the desired target dose.
Complete parameters are to be detailed in the corresponding TID Irradiation Test Plan.

5.4.11. Single Event Effects Radiation Tests

This activity will be managed by the end-user.

The Supplier shall provide the end-user with the parts quantity indicated in Figure 2 plus at least 2 control samples.

Device shall be characterized using specification defined in [AD6]. The purpose of this chapter is to define the requirements for the testing of the component for SEE arising from irradiation by energetic heavy ions.

5.4.11.1. SEE EFFECTS FORESEEN

Single Event Latch up
A permanent and potentially destructive state of the device under test whereby a parasitic thyristor structure is triggered by an ion strike and a low impedance, high current path is created.

Single Event Upset (SEU) and multiple SEU (MBU)
The change of state of a latched logic cell from one to zero or vice-versa. A single event upset is non-destructive and the logic element can be rewritten or reset.

The device architecture shall be analysed to identify functional blocks containing bistable elements such as registers or memory cells.

Test hardware and software shall be designed to allow the monitoring of functional blocks, together with the possibility of writing different patterns (e.g. all zero's, all one's, checker board, random pattern, etc.) and the re-writing of an affected cell after an SEU. The test software shall be capable of logging the number of upsets, the location and the time. It shall be capable of identifying and logging MCU and MBU.

A device may well contain a number of bistables of different design, each having a different single event sensitivity. Test coverage should be such as to allow these different sensitivities to be identified.

Single Event Functional Interrupt
A soft error that causes the component to reset, lock-up, or otherwise malfunction. SEFI typically occur in complex devices with built-in state/control sections like in modern memories

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(SDRAM, DRAM, NOR- and NAND-Flash, etc.), all types of processors, FPGAs or ASICs, or mixed-signal devices. Two main types of SEFI are distinguished depending on the actions required to restore operability : reset by software or by power cycling. The stored data may or may not be lost.

The SEFI sensitivity depends on the device operating mode. The device shall be tested in all operating conditions potentially encountered in applications. Test hardware and software shall be designed for the detection, logging and correction of all SEFI types. This includes software programming flexibility and hardware capability for reset and power cycling.

Single Event Transient
A temporary voltage excursion (voltage spike) at a node in a logic, or linear, integrated circuit, caused by a single energetic particle strike.

Analogue and mixed analogue/digital ICs may generate false outputs or transients as the result of SEE. Due to the fact that the bias, and input and output load conditions, significantly impact both the device SET sensitivity and characteristics, the device shall be tested either in worst-case or in the application conditions. The test system shall be capable of monitoring and logging these single event transients. The polarity (positive or negative), waveform, duration and amplitude of the transients shall be recorded.

The beam flux shall be sufficiently low so that the risk of SET pileup is minimum. SET pileup shall be discarded or analysed separately by post-irradiation software analysis.

5.4.11.2. SEL SETUP

During the SEE test campaign, a system for SEL detection/protection shall be used. It is a usual equipment owned by the companies used to run such SEE campaigns. The following paragraph is describing the system owned by Thales Alenia Space Spain.

5.4.11.3. THE THALES ALENIA SPACE CLARK SYSTEM

For SEL detection/protection of the DUT, Thales Alenia Space Spain has developed a SEU/SEFI test bench based on a Laptop. The Laptop configures the DUT registers (when applicable), and selects one of the up to DUTs to be tested. The SEL detection/protection system continuously monitors the current of the DUT and all the data are downloaded and saved in real time in the laptop.

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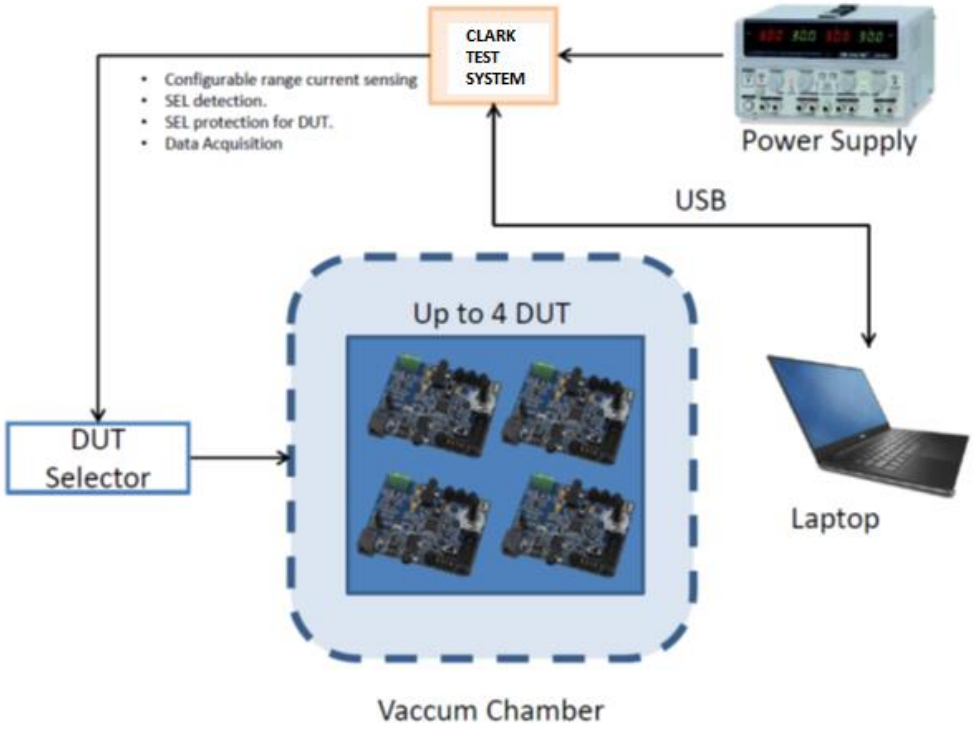

Figure 5 - CLARK System overview

The current is constantly monitored and in case of overconsumption the power supply output is automatically self-disabled. The acquisition system restarts again the power supply.

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Figure 6 - CLARK System in operation

The power supply is configured by the acquisition system. Voltage needs to be adjusted for each component or power rail to maximum Power Supply and the threshold current limit is set adequate for each. The acquisition system is constantly registering all of the current signals during each level of irradiation. If an event provokes an increase of the consumed current, the power supply disables the output automatically and the acquisition system restarts again the power supply after 100ms. For complex devices such as FPGAs, the power rail is grounded completely in order to avoid damage.

A data post-processing is performed afterwards in order to count the number and nature of the events.

A hot air gun is used to set the DUT temperature to Tjmax during SEL Testing. Temperature is continuously monitored by a thermal camera (see image).

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5.4.11.4. SEE TESTS SETUP

According to [RD2], the PROMISE circuit architecture shall embed as much as possible Built-In Self Test (BIST) structures for elements such as registers or memory cells. Test hardware and software shall be designed to allow the monitoring of BIST structures and functional blocks, together with the possibility of writing different patterns (e.g. all zero's, all one's, checker board, random pattern, etc.) and the re-writing of an affected cell after an SEU. The test software shall be capable of logging the number of upsets, the location and the time. It shall be capable of identifying and logging MCU and MBU.

A device may well contain a number of bistables of different designs, each having a different single event sensitivity. Test coverage should be such as to allow these different sensitivities to be identified.

5.4.11.5. SEE TESTS SEQUENCE

Two different campaigns are foreseen to complete both the device evaluation. Each campaign must be prepared with a dedicated SEE Irradiation Test Plan, that will contain all the details to perform the testing (functions to test, set-up, rates, samples, etc).

The first campaign will determine the SEL threshold for the device at high temperature (normally performed in the worst case operations at Tjmax and some basic elements.
The second campaign shall validate the IPs functions.

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6. VENDOR SURVEILLANCE

The end-user reserves the right to inspect at any time the components processed for qualification purposes.

The end-user shall be notified at least 2 working weeks in advance of the date of availability for Precap CSI and Final CSI in the end of qualification activities (TBC).

Once the Purchase Order is confirmed, the Supplier will send to the end-user, every 4 weeks, an updated activity progress report.

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7. QUALIFICATION TEST REPORT

A qualification test report shall be established. This report shall comprise the following :

- Cover sheet
- List of equipment (testing and measuring)
- List of test references
- Samples identification
- Samples production data
- Inspection data
- Initial electrical measurements data
- Construction Analysis data
- ESD characterisation data
- High Temperature Operating Life data
- NVM Data Retention test data
- NVM Endurance test data
- Radiation Tests data
- Control samples data
- Reserve samples data

[AD1] may be used as a guideline for content of this report.

This documentation shall be provided in electronic form.

The above shall be briefly reviewed as a summary of results and conclusion, indicating the success or otherwise of the qualification test plan.

Any production screens that need to be introduced for further production of Flight Models ASICs shall be outlined.

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8. QUALIFICATION OF PROMISE ASICS

As mentioned in para. 4, new IPs and new ASICs will be designed after the PROMISE project, using the PROMISE ecosystem.

The successful completion of this Qualification Plan on the PILOT Circuit will allow the users to safely limit the qualification effort of their own designs.

8.1. DIE-RELATED QUALIFICATION

Die-related qualification may be performed in accordance with [AD2] requirements.

The radiation topic will need to be processed specifically, depending on the radiation test results of this Qualification Plan, on the basic structures implemented in new IPs, and on the mission profile of the project using the newly designed ASIC.

8.2. PACKAGE-RELATED QUALIFICATION

Package-related qualification is out of the scope of the Pilot Circuit Qualification Plan ; that is why the Pilot Circuit is packaged into a well-known ceramic package.

For future ASICs production, in the case of a ceramic package, [AD2] will be the applicable standard.

If a plastic package in chosen, no ESCC standard is available at the moment (COTS standards are not relevant for specifically designed components).
A Working Group is actually preparing a new Generic Specification based on [AD2], currently named “ESCC9000P”, aiming at covering plastic packaged components for Space use.

Additionally, a new version of [AD1] will be written, allowing to have a complete coverage for Evaluation and Qualification of plastic-packaged devices.

8.3. FLIGHT MODELS PRODUCTION

For Flight Models production, [AD2] is the applicable document for components assembled in ceramic package.

The new “ESCC9000P” standard will be applicable for components assembled in plastic package.

These documents define the controls to be implemented during production and the screening to be applied.

Regarding screening, particular care shall be given to NVM.

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Depending on the chosen type of NVM, a specific screening aiming at guaranteeing the Data Retention at individual cells level may be necessary.

END OF DOCUMENT

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