PROMISE

WP3 Supply Chain Definition
D3.1 Manufacturing Plan Standard

Written by	***Responsibility*** + handwritten signature if no electronic workflow tool
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PUBLIC DOCUMENT

CHANGE RECORDS

ISSUE	DATE	§ CHANGE RECORDS	AUTHOR
001	12/03/2020	First version	M. Carquet
002	19/04/2020	Final version after reviews for submission	M. Carquet and F. Veljković

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1. PURPOSE

It is here after reminded the purpose of Task 3.1 of Work Package WP3 "Supply Chain Definition", as described in the Grant Agreement Number 870358 – PROMISE – H2020-SPACE-2018-2020 / H2020-SPACE-2019.

> Task 3.1: Define Manufacturing Plan Standard (M1-M3) - Leader: TASF - Participants: IMEC
> In this task, TASF shall define a standard manufacturing plan to be applied when building a PROMISE IPs based Mixed-Signal ASIC. This plan shall fix all the actors and processes needed along the supply chain as well as the requirements they need to comply in order to guarantee final performances and space-worthiness of the manufactured ASIC. In the same way, the quality controls to be performed during the production phase shall be defined.
> The Manufacturing Plan Standard documentation shall be issued as task output and the review corresponding to milestones shall be held.
> The related documentation shall be provided to TASF for future use by End-user.

Per this purpose, the present document is the Deliverable Number D3.1 "Manufacturing Plan Standard".

It will be used as an input for the WP3 Task 3.3 "Identify European actors space Mixed-signal ASIC supply chain".

Thales Alenia Space has the end-user role in the PROMISE consortium. Accordingly, during the PROMISE project, Thales Alenia Space will use this Manufacturing Plan as a support to issue a Procurement Specification dedicated to the PROMISE PILOT Circuit (Deliverable D4.2 of WP4 "Pilot Circuit Manufacturing"). The PILOT Circuit is handling the qualification at silicon level for the PILOT Circuit itself and for each embedded IP.

This Manufacturing Plan standard may help an end-user in issuing a Procurement Specification dedicated to his circuit designed using PROMISE library and ecosystem.

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2. RELATED DOCUMENTS

2.1. APPLICABLE DOCUMENTS

None

2.2. REFERENCE DOCUMENTS

Internal code / DRL	Reference	Title	Location of record
RD1	870358	Grant Agreement Number 870358 – PROMISE – H2020-SPACE-2018-2020 / H2020-SPACE-2019	
RD2	ESCC Generic Specification No 9000 – ESA document	Integrated Circuits : Monolithic and Multichip Microcircuits, Wire-Bonded, Hermetically Sealed and Flip-Chip Monolithic Microcircuits, Solder Ball Bonded, Hermetically and Non-Hermetically Sealed and Die	
RD3	ESCC Basic Specification No. 2049000 – ESA document	Internal Visual Inspection of Silicon-Based Non-Microwave Integrated Circuits	
RD4	PROMISE D1.1	Standard for Mixed-Signal IP Cores Design	

When no issue is mentioned, the relevant issue shall be the one in effect on the date of starting the components manufacturing or of placing the Purchase Order.

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2.3. ACRONYMS AND ABBREVIATIONS

ASIC : Application Specific Integrated Circuit
CSI : Customer Source Inspection
ESA : European Space Agency
ESCC : European Space Components Coordination
IO : Input Output
IP : Intellectual Property
ITP : Irradiation Test Plan
LAT : Lot Acceptance Test
MLM : Multi Layer Mask
MPW : Multi Project Wafer
PID : Process Identification Document
RFQ : Request For Quotation
ROM : Rough Order of Magnitude
SEE : Single Event Effect
SLM : Single Layer Mask
SWOT : Strengths, Weaknesses, Opportunities, Threats
TBC : To Be Confirmed
TBD : To Be Defined
TID : Total Ionising Dose
WP : Work Package

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3. GENERAL

The purpose of this document is to identify the activities and actors involved in the industrialisation and the procurement of a Mixed-Signal ASIC, starting “from scratch”.

PROMISE technology platform and libraries are not supporting Flip-Chip capabilities. So, only Wire Bond die connection is considered here.

The technology for PROMISE circuits has been chosen during the PROMISE project building.

The chosen technology is the X-FAB’s XH018, which offers a wide coverage of mid-range mixed signal circuit features, and availability of MPW, MLM and SLM reticles.

X-FAB is a European company, the foundry for the XH018 being located in Europe, in Corbeil-Essonnes, France.

Accordingly, there is no choice for the wafers manufacturer and foundry location, and the technology options are described in [RD4].

The PROMISE project will create a first set of IPs library validated by the PILOT Circuit and will set up an ecosystem to support new circuits design, and newcomers as IP providers. Access to PROMISE design capabilities will be fully supported by the activities of the WP6 “Exploitation, Dissemination & Networking”. Accordingly, the IP and circuit design aspects are out of the scope of this document.

This work can be split into 3 phases :

- selection of the supplier,
- development phase,
- production phase.

Industrialising and manufacturing an ASIC is a multifunctional work, involving different skills.

An overview is given in Table 1 here below.

This table gives a generic view.
Depending on the organisation of the End-user Company willing to develop the ASIC, the distribution of the activities may be different.

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Task	Subtask	Parts Engineer	Buyer	Technology Engineer	ASIC Designer	Radiation Engineer	Supplier	Auditor
Selection of the Supplier	Search for potential suppliers	✓	✓					
	Requests for quotation	✓	✓		✓			
	Short list	✓	✓					
	Technical visits	✓	✓	✓				
	Supplier final choice	✓	✓	✓				
	Audit	✓						✓
Development Phase	Package co-design	✓		✓	✓		✓	
	Support to the reticle design	✓			✓		✓	
	Test and Burn-In socket choice or design	✓			✓		✓	
	Test programme and fixtures	✓			✓		✓	
	Burn-In configuration	✓			✓		✓	
	Procurement Specification writing	✓			✓		✓	
	Process Identification Document writing	✓		✓			✓	
	Project management	✓						
Procurement Phase	Kick-off meeting	✓	✓				✓	
	Flight models production follow-up	✓	✓				✓	
	Precap CSI	✓					✓	
	Final CSI	✓			✓		✓	
	Lot acceptance tests	✓					✓	
	Data package review / Final lot acceptance	✓			✓			
	Radiation analysis and tests	✓			✓	✓		

Table 1 : Tasks and actors

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4. SELECTION OF THE SUPPLIER

4.1. SEARCH FOR POTENTIAL SUPPLIERS

The Parts Engineer and the Buyer shall share their knowledge of the European Space suppliers market, based on their participation in ESA Working Groups, conferences, exhibitions, etc.

As Task 3.3 of the WP3, Thales Alenia Space France will perform such a survey for the supply chain of the PILOT Circuit.

The PILOT Circuit will be assembled in a ceramic package.

4.2. REQUESTS FOR QUOTATION

The identified potential suppliers shall be asked to prepare a proposal based on a RFQ issued by the End-user.

At this step, definition of the needs may not be completely frozen, so the quotation may not be including a supplier's commitment.

The RFQ should list, as much as possible, the following elements :

- context of the project : ASIC for Space use,
- silicon technology implemented : XH018,
- main analog and digital functions, with basic performance description of each of them,
- estimated die size, bonding pad dimensions,
- type of package foreseen, and estimated number of IOs of this package,
- entity in charge of wafers procurement, wafer size,
- activities included/excluded (e.g. wafers procurement),
- number of devices for Engineering Models, Flight Models, unlidded SEE test devices, etc,
- screening and qualification flow,
- project schedule.

4.3. SHORT LIST

An analysis of all the received ROMs should lead to a short list of possible or preferred suppliers.

For this purpose, should be compiled to the maximum possible extent in the context of ROM quotations :

- the compliance of each of the proposals to the technical requirements,
- the compliance of each of the proposals to the schedule requirements,
- the technical heritage,
- the qualification status,

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- the financial analysis,
- the risk analysis, both technical and financial,
- the contractual aspects (e.g. Terms and Conditions), payment plan,
- the Export Control constraints,
- the customer relationship.

A SWOT analysis may be useful as a support to offers comparison.

4.4. TECHNICAL VISITS

Following completion of the previous activity, a technical visit should be requested to the short listed suppliers.

The purpose of this visit is to confirm, detail and complement the information presented in the ROM.

Space background of the potential supplier must be checked through examples of previous realisations.

A visit of the premises may allow to draw an opinion on the available technical means. Attendance of a Technology Engineer is recommended.

The basic processes and capabilities used by the supplier for Space components assembly shall be identified :

- wafer sawing,
- die gluing,
- die bonding,
- package sealing,
- other processes if plastic packaging is requested,
- packaged parts electrical test, probe test,
- burn-in,
- thermal and mechanical tests.

The use of external subcontrators shall be identified.
A one-stop-shop approach may be considered a plus, as it avoids the dilution of responsibilities.

Based on this, technical gaps to the achievement of the foreseen procurement of the ASIC shall be identified, either for assembly, test and screening, and qualification.

4.5. SUPPLIER FINAL CHOICE

Following the technical visits, the analysis of the ROMs may be refined and completed.

As a minimum, the final choice process should involve :

- the Parts Engineer,

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- the Buyer,
- the Technology Engineer.

The Project Manager and the Technical Authority may be invited.

4.6. AUDIT

After the choice of the Supplier is achieved and this Supplier has been notified, it is highly recommended that a formal audit is performed by a certified Auditor.

This audit should address the industrial maturity of the Supplier :

- verify as soon as possible the industrial capability vs the End-user requirements (product quality, supply chain, …),
- verify that the Supplier's industrial processes are stable and under control, so that the performance objectives can be achieved,
- a particular attention should be paid to the management of the relations between different premises of the Supplier if applicable, and to the management of the subcontractors if any,
- the audit shall be based on facts, figures and evidences, not only on procedures. It is recommended that the Parts Engineer participate in the audit, so that the validity of the presented technical content can be assessed.

A report shall be written, and signed by both parties.

An action plan, listing the corrective actions to be conducted, shall be established, and answers to the actions shall be monitored until they all are completed.

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5. DEVELOPMENT PHASE

It is important to point out that, particularly in the context of the design of a Mixed-Signal ASIC out of the frame of any official Qualification, the work of the ASIC Designer is in no way completed at tape-out.

The ASIC Designer will then be involved in several activities that can represent hundreds of hours of work and will last for months.

The availability of the ASIC Designer for these tasks must be taken into account in his workload.

5.1. PACKAGE CO-DESIGN

The ASIC being, by definition, a specific component, it is highly likely that no standard package will fit the need.

A standard package drawing may be used as a basis, and adapted to the ASIC die layout and constraints (cavity size, routing of differential signals, shielding of critical paths, power and ground planes, etc) .

Care shall be taken to the maximum bond length qualified by the Supplier for Space components.

The criteria for bond position inspection listed in [RD3] shall be taken into account for package cavity and die pad ring design, in order to minimize the yield loss at visual inspection.

Design of a specific cavity may be an opportunity to add the package internal routing to connect the lid to the relevant ground bias.

The ASIC Designer shall prepare a packaging specification.

This specification shall include :

- the die dimensions,
- the minimum pad pitch,
- the pads dimensions,
- the number of pads,
- the pad/pin correspondence, pads allocation die side by die side, including specific requirements if any (pad to be electrically connected to the seal ring, double bond need, physical separation of voltage domains, etc),
- the preliminary bonding diagram,
- the X-Y coordinates of the pads centers,
- the die orientation.

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5.2. SUPPORT TO THE RETICLE DESIGN

The wafer sawing process that the Supplier plans to use may drive a specific scribeline design (called by X-FAB “Reticle frame design”) to avoid residues of metallisation at the die edges, and so minimize the yield loss at visual inspection (see [RD3] for reference).

5.3. TEST AND BURN-IN SOCKET CHOICE OR DESIGN

Depending on the package chosen or designed, a standard socket may or may not be available for electrical test and burn-in.

The ASIC Designer is the Supplier’s contact point to correctly take into account any technical constraint, i.e. :

- a specific performance sensitivity,
- the estimated power dissipation.

5.4. TEST PROGRAMME AND FIXTURES

Following completion of the ASIC design phase, the ASIC Designer shall prepare for the Supplier a test specification.

This specification shall include :

- a block diagram,
- the by-default configuration (biasing, clocks, etc),
- the functional test patterns (SCAN, BIST, etc),
- for each block test : specific configuration (biasing, input signals, etc), list of parameters to be measured, expected lower and upper limits, measurement accuracy, etc.

It is highly recommended that, after the Supplier analysed the test specification, a face-to-face meeting is organised between the Supplier’s Test Engineer and the ASIC Designer, to allow for a detailed discussion on all the requirements and ensure their complete mutual understanding.

During the whole test software and hardware development phase, including probe test, the ASIC Designer is the designated contact point to the Supplier.

5.5. BURN-IN CONFIGURATION

The ASIC Designer shall provide the Supplier with a Burn-In electrical configuration specification.

This specification shall include :

- the biasing of the component, detailed for each block,
- the input signals to be applied,
- the power-on and power-off sequences if applicable.

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5.6. PROCUREMENT SPECIFICATION WRITING

The Parts Engineer is in charge of writing the Procurement Specification.

This Procurement Specification should preferably be based on the established ESCC9000 ([RD2]) format.
To our knowledge, no ESA document defines this format, so existing ESCC9XXX specifications should be used as examples (these specifications are available at the following address : https://escies.org/specfamily/view).

Writing of this specification should be started early in the development, and improved in an iterative way along the development process.

Regarding the ESCC9000 screening and qualification flows, all the deviations shall be listed in the Procurement Specification. In particular, some items, as some NVM technologies, may require specific screening and/or qualification operations.

In the case of a ceramic package, [RD2] shall be the applicable standard.
If a plastic package is chosen, no ESCC standard is available at the moment (COTS standards are not relevant for specifically designed components).
A Working Group is actually preparing a new Generic Specification based on [RD2], currently named “ESCC9000P”, aiming to address plastic packaged components for Space use.

The Procurement Specification shall specify the order of precedence of documents, by decreasing priority :

- the Purchase Order,
- the Procurement Specification,
- the Applicable Documents,
- the Reference Documents,
- other documents.

The Procurement Specification shall be frozen before starting Flight Models production.

It shall be kept under configuration control by the End-user.

It is recommended that a paper copy is countersigned by the Supplier, to acknowledge his commitment.

5.7. PROCESS IDENTIFICATION DOCUMENT WRITING

The Supplier is in charge of writing a Process Identification Document (PID), which shall completely describe how the ASICs will be manufactured, from raw materials procurement to delivery to the End-user.

The PID shall comprise, as a minimum :

- the suppliers list,

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- the involved technologies list,
- the constituent elements list,
- the applicable and reference documents list,
- the detailed assembly process flow, with applicable specifications references, and in-process controls (including sample size, AQL or LTPD, etc),
- the production, test and inspection equipment list,
- the package outline drawing,
- the bonding diagram,
- the lid marking,
- the screening flow, with applicable methods and conditions,
- the lot acceptance test flow, with applicable methods and conditions.

The PID shall be frozen before starting Flight Models production.

It shall be kept under configuration control by the Supplier.

A copy of the configured document shall be sent to the End-user.

5.8. PROJECT MANAGEMENT

The Parts Engineer is acting as a Project Manager during the whole process.

He is the interface between the different skills involved on the End-user side, and the contact point for the Supplier when discussing with the End-user.

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6. PROCUREMENT PHASE

6.1. KICK-OFF MEETING

Once the Purchase Order is placed, a kick-off meeting should be held at the Supplier's premises.

Objectives of the kick-off meeting are :

- review of the Procurement Specification issued by the End-user,
- review of the Process Identification Document issued by the Supplier,
- review of the schedule,
- etc.

6.2. FLIGHT MODELS PRODUCTION FOLLOW-UP

After the Flight Models production starts, the Supplier shall keep the End-user updated on the Work In Progress on a regular basis.
The periodicity of the updates shall be agreed by both parties.

Should a major issue occur during assembly, testing, screening or qualification, the Supplier shall notify the End-user by any appropriate written mean within 5 working days.
No further testing or analysis shall be performed until so instructed by the End-user.

6.3. PRECAP CSI

If stipulated in the Purchase Order, the End-user or his designated representative shall have the right of access to the Supplier's plant in order to perform the Pre-Encapsulation (Precap) Customer Source Inspection.

The required period of notification shall have been agreed by the parties.

The End-user shall advise the Supplier of his attendance, or attendance of his representative, and shall inform the Supplier of the inspections to be performed or witnessed.

6.4. FINAL CSI

If stipulated in the Purchase Order, the End-user or his designated representative shall have the right of access to the supplier's plant in order to perform the Final Customer Source Inspection (in the end of screening and/or end of Lot Acceptance Tests).

The required period of notification shall have been agreed by the parties.

The End-user shall advise the Supplier of his attendance, or attendance of his representative, and shall inform the Supplier of the inspections to be performed or witnessed.

It is recommended that the End-user asks the Supplier to send him the electrical test results prior to the Final CSI, so that the ASIC Designer can analyse them.

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6.5. LOT ACCEPTANCE TESTS

In the case of a ceramic package, [RD2] shall be the applicable standard.

If a plastic package is chosen, no ESCC standard is available at the moment (COTS standards are not relevant for specifically designed components).
A Working Group is actually preparing a new Generic Specification based on [RD2], currently named “ESCC9000P”, aiming at addressing plastic packaged components for Space use.

6.6. DATA PACKAGE REVIEW / FINAL LOT ACCEPTANCE

[RD2] may be used as a reference for the content of the Data Package.

The data documentation package shall be provided in electronic form.

Final lot acceptance may only be decided after delivery of the complete Data Package and successful review by the End-user.

6.7. RADIATION ANALYSIS AND TESTS

The radiation topic will need to be processed specifically, depending on the radiation test results of the PROMISE Qualification Plan applied to the PILOT Circuit, on the basic structures implemented in new IPs if any, and on the mission profile of the Project using the newly designed ASIC.

The ASIC Designer shall participate in the preparation of the test plans by the Radiation Engineer, either for TID or SEE tests, and it is recommended that he attends the SEE tests to leverage its design knowledge in the understanding of the observed ASIC behaviour.

END OF DOCUMENT

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