PROMISE

WP1 IPs Library and Pilot Circuit Specification

D1.1 Standards for Mixed-Signal IP Cores Design

Written by	***Responsibility*** + handwritten signature if no electronic workflow tool
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1. INTRODUCTION

1.1. SCOPE

The first steps in PROMISE WP1 are devoted to set the frame of the IP portfolio that will be made available for the Space Community. This is the first Pillar of the PROMISE vision.

This document is the "Standards for Mixed-Signal IP Cores design" to support the design activities for IPs and for Pilot Circuit in the frame of PROMISE project, to allow IP reuse and new IP and circuit design development after the project using the PROMISE library. The Design standard defines all the requirements that must comply the IPs to be included in the PROMISE library. It also includes all the design flow and recommendations to guarantee the accessibility and easy reuse of those IPs.

This document will evolve during the lifespan of the project and a final version will be issued by the end of the PROMISE project including all the Return of Experience.

1.2. APPLICABLE DOCUMENTS

Internal code / DRL	Reference	Version	Title
AD1	ECSS-Q-ST-60-02C	July 2008	Space Product Assurance-ASIC and FPGA development
AD2	D1.3 Interface Standards and IP Usage definition		PROMISE Interface Standards and IP Usage definition
AD3	DSFCL_HowTo-Analog_conventions.pdf		ANALOG CONVENTIONS

1.3. REFERENCE DOCUMENTS

Internal code / DRL	Reference	Title
RD1	ECSS-Q-HB-60-02A	Techniques for radiation effects mitigation in ASICs and FPGAs handbook
RD2	8.0.1, 2019-07-17	Xh018-ProcessSpecification

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Internal code / DRL	Reference	Title
RD3	D2.1 – IO cells Datasheet	IO cells Datasheet
RD4	D1.2 - Primitive list	Authorized and Forbidden Primitive list
RD5		XFAB EDA partners
RD6	D1.2 – POR requirements specification	POR requirements specification
RD7	D2.1 – Standard cells Datasheet	Standard cells Datasheet

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1.4. DEFINITIONS AND ACRONYMS

ASIC	Application Specific Integrated Circuit
ASSP	Application Specific Standard Products
BG	Bandgap
BIST	Built-In-Self-Test
CMOS	Complementary Metal-Oxide Semiconductor
DFT	Design For Test
DICE	Dual Interlocked Cell
EDA	Electronic Design Automation
ELT	Enclosed Layout Transistors
ESD	Electrostatic Discharge
FF	Flip-Flop
GDSII	Graphic Database System Information Interchange
GEO	Geostationary
HV	High Voltage
IO	Input and Output
IP	Intellectual Property
LET	Linear Energy Transfer
LVDS	Low Voltage Differential Signaling
MBIST	Memory BIST
MBU	Multiple Bit Upset
MOS	Metal Oxide Semiconductor
MV	Middle Voltage
NVM	Non Volatile Memory
PCM	Process Control Monitoring
POR	Power On Reset
RHBD	Radiation Hardening By Design
RTL	Regiter Transfer Level
SEB	Single Event Burnout
SEE	Single Event Effect
SEFI	Single Event Functional Interrupt
SEGR	Single Event Gate Rupture
SEL	Single Event Latchup
SET	Single Event Transient
SEU	Single Event Upset
TID	Total Ionization Dose
WP	Work Package

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1.5. DOCUMENT OUTLINE

Section 1 describes the purpose, scope and application field of this document. In addition, it gives useful information for a better understanding of the document such as applicable documents, reference documents, specific definitions used or refer to in the document and at least the list of acronyms used. A brief presentation of its content completes this section.

Section 2 describes the format and wording standard for the IP and circuits requirement specification documents.

Section 3 describes the environmental requirement. It covers power supplies description, thermal environment and a radiation environment chapter describes all requirement for each type of radiation effects.

Section 4 describes the technology options, metal layers and related technology modules to ensure that all the IPs are consistent to be embedded on the same silicon chip. All the authorized primitive devices are listed in accordance to the selected modules and their space environment withstanding.

Section 5 describes the design rules by covering the simulation corners, the padring strategy, recommendations for digital and analog design, recommendations for layout. Guidelines for interfaces and testability constraints is providing a common approach for testability implementation that will ease the test house test program implementation in the frame of PROMISE community. The typical power-up sequence is described as well as naming convention to ensure consistency across the hierarchy and a fluent integration with other IPs and top-level design.

Section 6 describes the design flow, the EDA tools constraints, provides some recommendation to anticipate design kit version update and recalls the mains guidelines for design methodology.

Section 7 describes briefly recommendation for design reviews according AD1 to ensure a secured and mastered design process and guaranty the higher level of design quality

Section 8 describes briefly the recommendations for design documentation.

Section 9 describes hardening guidelines covering SEL, TID, SET and SEU effects.

Section 10 describes high level guidelines for IP data package and sanity check in relation with AD2.

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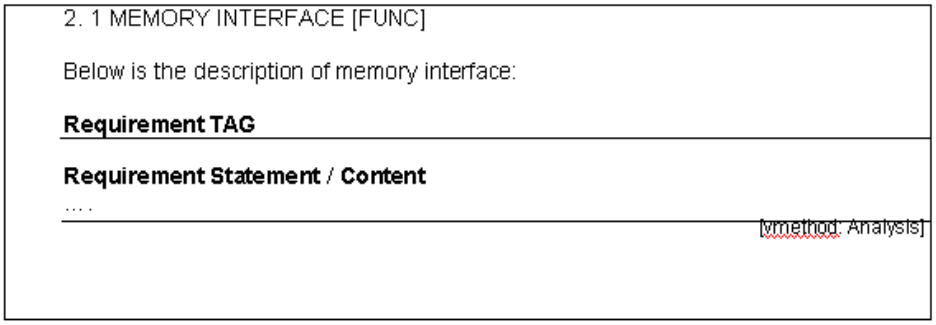
2. REQUIREMENTS SPECIFICATION WORDING [REQW]

Requirement DS-REQW-01 :

The following paragraphs are defining format and wording standard for the IP and circuits requirement specification documents :

2.1. FORMAT

Requirements format is:



Requirements TAG have format: **REQ-BLOCK-FUNC-0001**

- **FUNC** is the keyword placed in [..] within the preceding title. It is supposed to describe the Functionality.
- Counter digit Number: **4**

Every **Requirement Statement / Content** is defined between 2 lines.

Verification method **(vmethod)**: specifies how the requirement has to be verified. One among the following:

Verification Method	Requirements targeted
Simulation	Functional or performance requirements
Analysis	Requirements non verifiable by simulation models. They can be covered by a data book reference or a tool log analysis.
Test	Requirement is verified only on prototype or during board validation.
Inspection	When all other verification method is not applicable.

Table 1 : Verification methods description

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2.2. WORDING

The text which is not labeled shall be considered as an explanation, which may be needed for better reader understanding and can help to clarify possible different interpretation, although it should be aimed that all requirements are worded as unambiguous, and verifiable.

The following requirement terminology and labeling conventions are used throughout this document:

Mandatory Requirement - This identifies a feature or function that is a firm and binding requirement of the product. Failure to meet a Mandatory Requirement may cause application restrictions, result in improper functioning of the product or hinder operations.

- A Mandatory Requirement contains the word “shall". Equivalent expressions for use in exceptional cases: is to, is required to, it is required that, has to, only ... is permitted, it is necessary.
- A Mandatory Requirement is not worded as: is not allowed [permitted] [acceptable] [permissible], is required to be not, is required that ... be not, is not to be, must not.

Desirable Requirement - This identifies a feature or function that is an optional but desirable feature.

- A Desirable Requirement contains the word “should". Equivalent expressions for use in exceptional cases: it is recommended that, ought to
- A Desirable Requirement should not: it is not recommended that, ought not to

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3. PROMISE ENVIRONMENT REQUIREMENTS

The following paragraphs are describing environmental requirements that are common to all design in the frame of PROMISE design eco-system..

3.1. POWER SUPPLIES [PWRS]

Requirement DS-PWRS-02 :

According AD3 naming convention, the power supplies name shall be :

VDD1V8 / VSS1V8
VDDIO3V3 / VSSIO3V3
AVDD1V8 / AVSS1V8
AVDD3V3 / AVSS3V3
VSUB for substrate PTAP contact

[vmethod: Analysis]

Requirement DS-PWRS-03 :

The Digital Core power supply VDD1V8 is 1.8V +/-10%

[vmethod: Simulation]

Requirement DS-PWRS-04 :

The Digital IOs power supply VDDIO3V3 is 3V3 +/-10%

[vmethod: Simulation]

Requirement DS-PWRS-05 :

The Analog power supply AVDD1V8 is 1.8V +/-10%

[vmethod: Simulation]

Requirement DS-PWRS-06 :

The Analog power supply AVDD3V3 is 3.3V +/-10%

[vmethod: Simulation]

Requirement DS-PWRS-07 :

The substrate connection (using PTAP) VSUB shall be handle like a power supply to ensure a low parasitic serial resistor to the GND substrate pads.

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3.2. THERMAL ENVIRONMENT [THEN]

Requirement DS-THEN-08 :

The block shall be functional between TJfuncmin=–40°C and TJfuncmax=125°C junction temperature and ensure cold start at TJfuncmin=–40°C junction temperature.

[vmethod: Simulation]

Requirement DS-THEN-09 :

Performance requirements shall be reached between TJperfmin=0°C and TJperfmax=+105°C junction temperature. (assuming a +20°C / W RTh-JC).

[vmethod: Simulation]

3.3. RADIATION ENVIRONMENT [RAEN]

The following radiation requirement can only be validated by test ; no tool is available in PROMISE to extract by simulation the radiation performances of the IPs. PROMISE IPs will use hardening by design approach, using hardening techniques described in RD1.

After SEE evaluation of the IPs on the Pilot Circuit, the available data will enable the analysis of event rates versus specific space mission profile. The space mission profile is defined by the end-user ; a typical GEO orbit spectra fluence is given as example in the following figure :

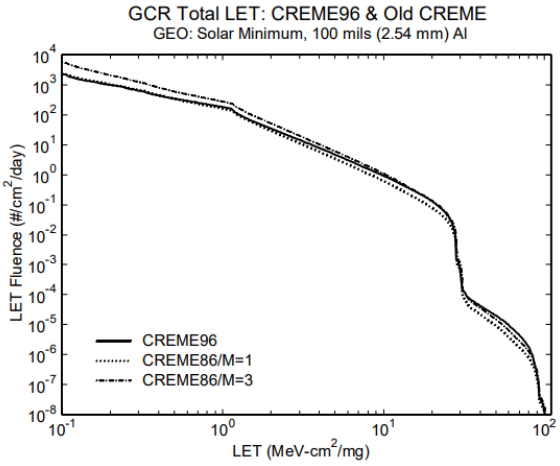

Figure 1 : Example of typical GEO orbit spectra fluence

3.3.1. TID

Requirement DS-RAEN-10 :

TID : the block shall be compatible with a 100krad minimum Total Ionizing Dose (TID).

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[vmethod: Test]

3.3.2. SEU

Requirement DS-RAEN-11 :

The SEU rate goal shall be less than 10^{-8} Ev/day/FF (or memory point) on GEO orbit while using Single Error Correction (SEC) and Double Error Detection (DEC).

[vmethod: Test]

3.3.3. SEL

Requirement DS-RAEN-12 :

SEL immune up to a LET of 60MeV.cm²/mg.

[vmethod: Test]

3.3.4. SEFI

Requirement DS-RAEN-13 :

SEFI immune up to a LET of 60MeV.cm²/mg (such as unwanted reset, loss of configuration, state machine jam or transition dead state).

[vmethod: Test]

3.3.5. MBU in memories

Requirement DS-RAEN-14 :

MBU immune up to a LET of 60MeV.cm²/mg.

[vmethod: Test]

3.3.6. SET

Requirement DS-RAEN-15 :

The SET error rate to reach for the block shall be less than 10^{-8} Ev/day/device on GEO orbit.

[vmethod: Test]

3.3.7. SEGR

Requirement DS-RAEN-16 :

For high voltage MOS transistors, the Safe Operating Area shall be defined to ensure SEGR immune up to a LET of 60MeV.cm²/mg.

[vmethod: Test]

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3.3.8. SEB

Requirement DS-RAEN-17 :

For high voltage MOS transistors, the Safe Operating Area shall be defined to ensure SEB immune up to a LET of 60MeV.cm²/mg.

[vmethod: Test]

4. TECHNOLOGY OPTIONS AND DESIGN KIT [TODK]

All technology documentation, design kit and EDA configuration are available on the XFAB web site http://my.xfab.com. RD2 includes a useful set of document covering :

- Design Rule Specification
- PCM Acceptance Specification
- Process and Device Specification
- Process Reliability Specification

Requirement DS-TODK-18 :

The latest version of documentation and design kit shall be downloaded from my.xfab.com.

[vmethod: Analysis]

4.1. DESIGN KIT INITIALIZATION [DKIN]

Requirement DS-DKIN-19 :

Design kit is configured using the XFAB xkit software. A PROMISE project shall be initialized using the following xkit initialization option :

Core Module:	1 - LP (Low Power 1.8V)
MOS Module:	1- MOS3 (3.3 Volt MOS)
METALS:	4 - 4 Thin Metals
TOPMETALS:	3 - Top and Thick Metal: METTP & METTPL
FINAL_CODE =	"1143"

[vmethod: Analysis]

4.2. METAL LAYERS [MELA]

The selected options are consistent with those available on XFAB MPW (6 Metal Layers: MET1-MET2-MET3-MET4-METMID-METTHK; MIM or MIMH are optional capacitor modules) and is a good trade-off between digital routing density, analog and power/high current capabilities.

Requirement DS-MELA-20 :

The PROMISE options are supporting the following metal stack only :

6 Metal Layers: MET1 - MET2 - MET3 - MET4 – METTP – METTPL

It corresponds to the module combination :

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MET1 - MET2 - MET3 - MET4 – METMID - METTHK

[vmethod: Analysis]

Thick metal is beneficial for analog/mixed-signal designs. Some drawback for purely digital designs is expected, although the top metals are mainly used for power routing.

The metal thicknesses and related performances are defined in RD2.

Requirement DS-MELA-21 :

DMIM capacitor module is selected to provide the best density, linearity and matching trade-off.

[vmethod: Analysis]

4.3. PRIMITIVE DEVICE LIST [PDLI]

The exhaustive list of available primitives in the XFAB XH018 technology platform is available in RD2.

Requirement DS-PDLI-22 :

The exhaustive list of authorized primitive devices for IP and circuit design in PROMISE is given in RD4.

[vmethod: Analysis]

Requirement DS-PDLI-23 :

The exhaustive list of primitive devices that shall not be used in IP and circuit design in PROMISE is given in RD4. They should be used only for evaluation purpose and shall not be re-used before being promoted to the authorized primitive devices list.

[vmethod: Analysis]

4.4. SELECTED PROCESS MODULES [SPMO]

Requirement DS-SPMO-24 :

The exhaustive list of process module for PROMISE circuit is given in RD4 according the authorized primitive list.

[vmethod: Analysis]

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5. DESIGN RULES

5.1. SIMULATION CORNERS [CORN]

The functional and performances temperature ranges are defined in the chapter 0

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Thermal environment [THEN] page 14.

Note : the process corners are predefined as follow for all devices:

tm → typical mean
wp → worst case power
ws → worst case speed
wo → worst case one
wz → worst case zero

Model Class	Parameter	wp	ws	wo	wz
MOS	NMOS	fast	slow	fast	slow
	PMOS	fast	slow	slow	fast
Bipolar Transistors	speed	high	low	-	-
	beta	high	low	-	-
Resistors	resistance	low	high	-	-
Diodes	capacitance	low	high	-	-
Capacitors	capacitance	low	high	-	-

These basic corner sets may be adapted to the design specific needs (bipolar in BG, etc…).

Requirement DS-CORN-25 :

The typical junction temperature TJtyp = 25°C.

[vmethod: Simulation]

5.1.1. Digital core corners

Requirement DS-CORN-26 :

PROMISE digital core corners are :
tm / VDD1V8typ/ TJtyp
+ (ws/wp X VDD1V8min/max X TJfuncmin/TJfuncmax)

Giving 1 + (2x2x2) = 9 corners for digital core cells simulations.

[vmethod: Simulation]

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5.1.2. Digital IOs corners

Requirement DS-CORN-27 :

PROMISE digital IOs corners are :
tm / VDD1V8typ / VDDIO3V3typ / TJtyp
+ (ws/wp X VDD3V3min/max X VDD1V8min/max X TJfuncmin/TJfuncmax)
1.8V and 3.3V are correlated.

Giving 1 + (2x2x1x2) = 9 corners digital IOs simulations.

[vmethod: Simulation]

5.1.3. Analog functional corners

Requirement DS-CORN-28 :

PROMISE analog functional corners are :

tm / AVDD1V8typ / AVDD3V3typ / TJtyp
+ (ws/wp X AVDD1V8min/max X AVDD3V3min/max X VDD1V8min/max X VDDIO3V3min/max X TJfuncmin/TJfuncmax)
1.8V and 3.3V are correlated.
Analog and digital supplies are correlated.

Giving 1 + (2x2x1x1x1x2) = 9 corners for analog functional simulations.

[vmethod: Simulation]

5.1.4. Analog performance corners

Requirement DS-CORN-29 :

PROMISE analog performance corners are :

tm / AVDD1V8typ / AVDD3V3typ / TJtyp
+ (tm/ws/wp/wo/wz X AVDD1V8min/max X AVDD3V3min/max X VDD1V8min/max X VDDIO3V3min/max X TJperfmin/TJperfmax)

Giving 1 + (5x2x1x1x1x2) = 21 corners for analog performance simulations, if all power supplies are correlated.

[vmethod: Simulation]

Requirement DS-CORN-30 :

Analog performance corners shall be adapted to the simulated circuit by including all other contributor as resistors, capacitors, etc…

[vmethod: Simulation]

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Requirement DS-CORN-31 :

Eventual non correlation between analog 1.8V and 3.3V and between analog and digital supplies shall be taken into account to define the corners.

[vmethod: Simulation]

Requirement DS-CORN-32 :

Analog performance drift range could be defined inside the performance range.

[vmethod: Simulation]

5.1.5. Digital Top-Level Sign-off corners

Requirement DS-CORN-33 :

Digital Top-Level Sign-off corners are :
tm / VDD1V8typ / VDDIO3V3typ / AVDD1V8typ / AVDD3V3typ / Ttyp
+ (ws/wp X AVDD1V8min/max X AVDD3V3min/max X VDD1V8min/max X VDDIO3V3min/max X Tfuncmin/Tfuncmax)
1.8V and 3.3V are correlated. Analog and digital are correlated.

Giving 1 + (2x2x1x1x1x2) = 9 corners

[vmethod: Simulation]

5.1.6. Monte-Carlo corners

Requirement DS-CORN-34 :

Monte-Carlo simulations shall be performed using at least 3 sigma dispersion for wafer lot dispersion and devices mismatch.

[vmethod: Simulation]

Requirement DS-CORN-35 :

For critical analog performances related to devices mismatch (offsets, bandgap voltages, etc…), it is recommended to run Monte-Carlo simulation using devices mismatch in combination with worst case corners.

[vmethod: Simulation]

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5.2. PADRING STRATEGY [PADR]

Requirement DS-PADR-36 :

Designer shall use the analog and digital pads available in the IOs libraries available for PROMISE. (cf RD3).

[vmethod: Analysis]

Nota : LVDS, power on controlled bidirectional IOs, analog IO, power supplies pads are part of the PROMISE IP design activities.

Requirement DS-PADR-37 :

For ESD performances and protection strategy, refer to RD3 and the ESD documentation on "my X-FAB".

[vmethod: Analysis]

Nota : HV and MV need specific ESD protection ; part of them could be used in the frame of HV MOS radiation evaluation in PROMISE Pilot Circuit.

Requirement DS-PADR-38 :

IMEC may provide some advises and basic tools to support padring design.

[vmethod: Analysis]

Requirement DS-PADR-39 :

The padring shall be defined using a .csv table including the following columns :

Side	Pad cell name	X coordinate	Y coordinate
North			
East			
South			
West			

The file may be used as a unique database to generate cell views (schematic, layout).

[vmethod: Analysis]

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5.3. DIGITAL DESIGN RECOMMENDATION [DDRE]

Timing margins shall be taken for digital design :

Requirement DS-DDRE-40 :

A 25ps margins shall be taken into account on hold timing to cover uncertainty on contributors.

[vmethod: Analysis]

Requirement DS-DDRE-41 :

Globally, a 10% margin shall be applied on the maximum clock frequency to cover setup margin, TID drift and an ageing margin that are not taken into account in .lib timings.

[vmethod: Simulation]

Requirement DS-DDRE-42 :

IMEC shall provide support to implement the digital power grid and common rules for digital placement and routing.

[vmethod: Analysis]

5.4. ANALOG DESIGN RECOMMENDATION [ADRE]

Requirement DS-ADRE-43 :

Never connect a low voltage (1V8) gates directly to a supply (power or ground). Dedicated tie cells must be used to prevent ESD stress on the thin gate of the transistor (cf RD7).

[vmethod: Analysis]

Requirement DS-ADRE-44 :

Never connect IO transistor gates directly to a supply (power or ground). Dedicated tie cells must be used to prevent ESD stress on the thin gate of the transistor (cf RD7).

[vmethod: Analysis]

Requirement DS-ADRE-45 :

If a clock is used between an analog IP and the digital core, it is recommended that the analog IP provides the clock for data synchronization to the digital core (even if the clock is initially provided by the digital core)

[vmethod: Analysis]

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Requirement DS-ADRE-46 :

The required views for an analog block in a digital flow are defined in AD2. Basically, a .lib file including all arcs in all modes and a simple .v (connectivity) are required.

For mixed-signal simulations of analog blocks, a .va (behavioral Verilog A model) is very useful. Such behavioral model can go from very simple to very complex. The designer should define clearly the limitations of the .va behavioral model in the IP datasheet. The main modes of the IP should be modeled. Correlation of the .va model with spice models is needed. Only the typical corner is enough for the .va model and the comparison.

[vmethod: Simulation]

Requirement DS-ADRE-47 :

Each analog IP shall be provided with a power down command.

[vmethod: Simulation]

Requirement DS-ADRE-48 :

The power-up and power-down sequences shall be simulated while verifying the Safe Operating Area.

[vmethod: Simulation]

5.5. LAYOUT RECOMMENDATION [LREC]

Requirement DS-LREC-49 :

A dedicated PIN named VSUB shall be used for substrate PTAP contact ; this VSUB pin is common to all IPs and is connected at top level to a dedicated PIN of the chip.

[vmethod: Analysis]

Requirement DS-LREC-50 :

All IPs shall have :

- a DNWELL or DNWELLMV ring at the periphery.
- a n+ ring + metal1 to contact the DNWELL or DNWELLMV to the related VDD supply.
- a wide substrate PTAP + metal1 ring around the IP, outside the DNWELL or DNWELLMV ring. This ring is connected via the PIN VSUB.

[vmethod: Analysis]

Requirement DS-LREC-51 :

The IP pins shall be defined at the IP periphery and its geometry shall correspond to the metal width to be connected.

[vmethod: Analysis]

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Requirement DS-LREC-52 :

The layout shall implement as much as possible contacts and vias.
A minimum of 2 vias or contacts shall be implemented in analog IPs.

[vmethod: Analysis]

Requirement DS-LREC-53 :

For internal analog IPs only, and when there is no impact on performances, a derating factor of 50% shall be taken regarding the current density parameters vs electro migration (wires, vias, contact).
For digital design, electro migration shall be consistent with XFAB rules without specific margin.

[vmethod: Analysis]

Requirement DS-LREC-54 :

To avoid missing connection at upper level, the connect-by-name option in LVS is forbidden at all level of hierarchy. Accordingly, interfaces of all supplies and interfaces shall be made using a unique pin.

[vmethod: Analysis]

5.6. INTERFACES CONSTRAINTS [INCO]

Requirement DS-INCO-55 :

Digital block shall be supplied by the unique digital core supply VDD1V8. Different digital core power domain are forbidden.

[vmethod: Analysis]

Requirement DS-INCO-56 :

Cross power domains (VDD1V8 from-to AVDD1V8, from-to VDDIO3V3, from-to AVDD3V3) shall be handled by the relevant level shifters inside the analog block.

PROMISE library provides cross domain level shifter with pull-up or pull-down behavior during power-on when the CORE VDD1V8 supply is not present (Power On Reset block output can be used). The level shifters include the proper ESD strategy at power domain change.

[vmethod: Analysis]

Requirement DS-INCO-57 :

To avoid glitches at digital outputs during power-on, the digital IO buffer with Power-On-Control system shall be used (Cf RD3).

[vmethod: Simulation]

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5.7. TESTABILITY CONSTRAINTS [TEST]

The testability constraints are defined to ensure a fluent integration with other IPs and top-level design and providing a common approach for testability implementation that will ease the test house test program implementation in the frame of PROMISE community;

5.7.1. Digital DFT

Requirement DS-TEST-58 :

The goal of digital Design For Test are :
- Scan stuck-at : coverage > 98%
- Memory BIST (at speed)
- Boundary scan

[vmethod: Simulation]

Requirement DS-TEST-59 :

The scan version of the hardened FF shall be SEU used.

[vmethod: Simulation]

Requirement DS-TEST-60 :

If registers are used to configure test mode, the related FF shall be SEU hardened and gated by primary pin of the circuit.

[vmethod: Simulation]

Requirement DS-TEST-61 :

For hard macros (i.e. all blocks having a layout view), the digital DFT shall be embedded with the IP. The required views and files are defined in AD2.
Note : All blocks designed in the frame of PROMISE project are hard macros.

[vmethod: Simulation]

Requirement DS-TEST-62 :

For soft macros (i.e. IPs at RTL level), DFT can be handled at top level if :
- All Clocks are controlable through dedicated bypass
- All asynchronous Reset are controllable through dedicated bypass
- All synchronous reset areindependent from asynchronous reset in scan mode

[vmethod: Simulation]

Requirement DS-TEST-63 :

All memories must be bypassed in scan mode.

[vmethod: Simulation]

Requirement DS-TEST-64 :

All bidirectional IOs shall be in a defined state during test mode.

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[vmethod: Simulation]

Requirement DS-TEST-65 :

Precaution must be taken for Memory BIST insertion : the number of MBIST controller shall be traded-off versus area and at speed capability.

[vmethod: Simulation]

5.7.2. Analog DFT

Requirement DS-TEST-66 :

The proposed strategy is to handle the analog multiplexing of all analog test signal at top level through a low bandwidth test connection dedicated to the 2 analog power domain (AVDD3V3 and AVDD1V8).

[vmethod: Simulation]

Requirement DS-TEST-67 :

The analog test switches shall be of T type : 2 serial MOS switches and in the middle a parallel MOS switch to the GND (to limit noise coupling across the test network). If the leakage current in the MOS to GND has impact on analog performances, this MOS may be connected to a voltage between GND and VDD.
The 2 serial switches shall have different digital command signal to contribute to SET mitigation.

[vmethod: Simulation]

Requirement DS-TEST-68 :

The switches control logic driver shall use SET free circuitry (cf SET hardening chapter).

[vmethod: Simulation]

Requirement DS-TEST-69 :

The top level digital core shall handle the control and decoding of all analog test switches. The decoder shall avoid any simultaneous command of different test switches.

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Requirement DS-TEST-70 :

All the analog test signal shall be connected in a daisy chain mode at top level to 2 differential pads per analog power domain :

- ana-testout_p_1V8 and ana-testout_n_1V8
- ana-testout_p_3V3 and ana-testout_n_3V3

[vmethod: Simulation]

Requirement DS-TEST-71 :

The tested signal shall not be disturbed by the analog test circuitry and remain in a known and representative state (no induced oscillation, etc…).

[vmethod: Simulation]

Requirement DS-TEST-72 :

If high bandwidth testability needs to be implemented, it shall be fully handled and implemented at IP design level independently to the standard low bandwidth testability.

[vmethod: Simulation]

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5.8. POWER-ON SEQUENCE [PWRO]

PROMISE circuit architecture power domains are defined in paragraph 3.1 Power supplies [PWRS] page 13.

Requirement DS-PWRO-73 :

A PROMISE circuit shall embed the Power On Reset block (cf RD6). An internal LDO may be used to generate the internal 1.8V from the external 3.3V supply.

[vmethod: Simulation]

Requirement DS-PWRO-74 :

Based on this architecture at circuit top level, the Power-ON sequence shall be :

- Power-on of the external 3.3V power supply
  - At power-on, the POR sets its reset output signals at “0”.
- When the 3.3V power supply voltage reaches the POR threshold, the POR rises 3V3_ready signal at “1”. POR reset output signals stays at “0”.
  - 3V3_ready signal is used as an enable to start the PROMISE BG and LDO 1V8 IPs :
    - The bandgap starts with initial trimming
    - The LDO1V8 generates the 1.8V supply from the 3v3 external power supply
- When the 1.8V supply voltage reaches the POR threshold, the POR set its reset output signal at “1”.
  - This reset signal is used by others IPs in PROMISE ASSP to release their reset state.
  - The circuit is operated nominally and the BG can be trimmed using digital interface or trimming code stored in the NVM.

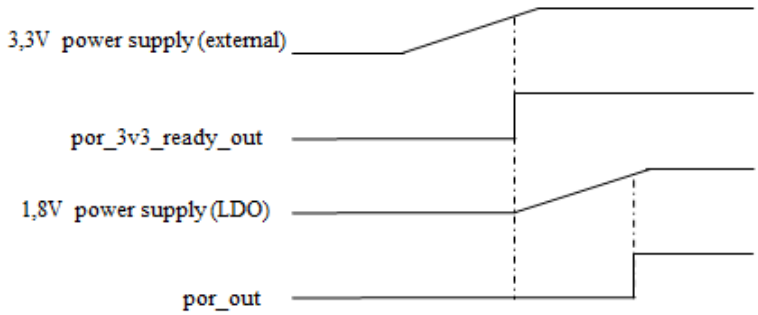

Figure 2 : Power-ON sequence

[vmethod: Simulation]

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5.9. NAMING CONVENTION [NACO]

Requirement DS-NACO-75 :

The pins type and direction (input, output, etc…) shall be defined and consistent across the design hierarchy.

[vmethod: Analysis]

Requirement DS-NACO-76 :

The naming conventions shall fulfill the requirements as described in AD3

[vmethod: Analysis]

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6. DESIGN PROCESS

6.1. DESIGN FLOW [DFLO]

Requirement DS-DFLO-77 :

The PROMISE circuit design flows options are described in AD2.

The baseline design flow for a digital, an analog or mixed circuit is Digital-on-top (i.e. digital P&R does the circuit top-level ; the design flow handles the design from RTL to GDSII).

Analog-on-top methodology can be used for pure analog circuit.

[vmethod: Analysis]

Requirement DS-DFLO-78 :

Mixed-signal or analog IPs useful views and data package to be integrated in the PROMISE library are described in AD2.

Some specific views to be handled by the digital P&R tool in a digital-on-top design flow require an additional design effort versus a usual analog full-custom design flow, but digital-on-top design flow ensures the highest level of intellectual property protection and the highest level of reusability.

[vmethod: Analysis]

Requirement DS-DFLO-79 :

All analog/mixed-signal IP must be simulated using the analog functional corners to extract the timing models. (Those corners are consistent with the digital corners to allow consistent digital-on-top design flow).

[vmethod: Simulation]

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6.2. TOOLS SET [TOSE]

XFAB supports tools from all major EDA companies for design with XH018 technology.

Requirement DS-TOSE-80 :

Due to limited knowledge of such tools at IMEC and to avoid any problem in case difference in IP simulation results, verification results, etc…, the tools set for final data package in PROMISE library is restricted to the tools defined in AD2.

[vmethod: Analysis]

Requirement DS-TOSE-81 :

Upon design house responsibility, a different design tool set can be used during the IP detailed design phase, but the IP data package shall be fully verified by the design house using the PROMISE tool set to be promoted to the PROMISE library.

[vmethod: Analysis]

6.3. DESIGN KIT VERSION UPDATE [DKVU]

Despite the XH018 is a very mature technology, the design kit has regular new version, mainly to introduce new features. But it can also be library updates e.g. a layout rule changes, a digital standard cell changes, a transistor model changes, etc…

Requirement DS-DKVU-82 :

It is highly advised to the IP design house to verify the impact of the new design kit version on its existing PROMISE IPs. At IP design level, a proper design and verification data organization may help to run with low effort a non-regression verification with a new XFAB design kit version.

[vmethod: Analysis]

6.4. DESIGN METHODOLOGY [DMET]

The design methodology shall follow the recommendation in AD1. For PROMISE design, it is proposed to stick to some simple recommendation to guaranty a high level of first time success : understood specification, accurate architecture analysis, exhaustive coverage of requirements by the simulation plan.

Requirement DS-DMET-83 :

Verify the good understanding of IP or Circuit requirement specification during the Kick-Off and Input Specification review. Identify all requirement that may be changed by the customer and the requirements that can be traded-off.

[vmethod: Analysis]

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Requirement DS-DMET-84 :

During the definition phase, in addition to the AD1 guidelines, clearly define the main architecture aspects that will drive the architecture analysis. These main architecture aspects shall be presented to the customer and agreed with him during the System requirement review.

[vmethod: Analysis]

Requirement DS-DMET-85 :

During the architectural design, in addition to the AD1 guidelines, the top level symbol shall be finalized, as well as the first floor plan defining the position of the interfaces. The behavioral model shall be created to start verifying the main functional requirements. It is important to also take into account all the testability and validation constraints at architecture level. The sub blocks detailed specification shall be also defined and included to the verification plan and compliance matrix in relation with the top level requirements.

[vmethod: Analysis]

Requirement DS-DMET-86 :

During the detailed design phase, in addition to the AD1 guidelines, the simulation plan shall be fully defined and implemented in the CAD tools in parallel of the schematic creation. The coverage of the requirements shall be exhaustively verified using the compliance matrix template provided in the circuit specification.
Only start the detailed devices sizing when simulation plan is fully implemented.

[vmethod: Analysis]

Requirement DS-DMET-87 :

The detailed layout shall be only started after the Detailed design review. To avoid any re-design / re--layout loops.

[vmethod: Analysis]

Requirement DS-DMET-88 :

The methodology shall be implemented at each level of the design ; for lower level blocks, the formalism can be reduced, but the philosophy shall be respected.

[vmethod: Analysis]

Requirement DS-DMET-89 :

For the top level design (IPs or ASIC), the methodology shall be 100% respected.

[vmethod: Analysis]

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7. DESIGN REVIEWS [DERE]

Requirement DS-DERE-90 :

A Kick-Off and Input Specification review shall be schedule at the very beginning of the design activities to assess the good understanding of all the items of the IP requirement specification.

[vmethod: Analysis]

Requirement DS-DERE-91 :

During the IPs and top level circuit design activities, the reviews defined in AD1 shall be held.

[vmethod: Analysis]

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8. DOCUMENTATION [DOC]

Requirement DS-DOC-92 :

The design documentation shall follow the recommendation in AD1. The content and the format will be designer-friendly oriented while fulfilling a high level of compliance with AD1.

[vmethod: Analysis]

Requirement DS-DOC-93 :

The Design documentation issued during the design phase of PROMISE IPs and Pilot Circuit may be used as template for future design activities (after removing non disclosable information).

[vmethod: Analysis]

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9. HARDENING RECOMMENDATIONS [HARD]

An exhaustive view of RHBD techniques is available in RD1. The purpose of this chapter is to define a subset of essential hardening technique that shall be used by PROMISE designer community to ensure the best compliance with the radiation requirements.

9.1. SEL HARDENING [SELH]

Requirement DS-SELH-94 :

The main mitigation for SEL in bulk CMOS technology is the use of systematic diffusion guardrings to separate NMOS from PMOS :

- NIMP/DIFF guardring at the periphery of NWELL
- PIMP/DIFF guardring at the periphery of PWELL

[vmethod: Analysis]

Requirement DS-SELH-95 :

Mixed signal-design are taking advantages in the use of triple-well (ISOMOS module). Each DNWELL area shall be implemented with :

- NWELL+NIMP/DIFF guardring at the periphery of the DNWELL
- PIMP/DIFF guardring around the DNWELL. This PIMP guardring is connected to the substrate.

[vmethod: Analysis]

Requirement DS-SELH-96 :

If ISOMOS module is not used, PIMP/DIFF guardring shall be implemented around the NWELL and NIMP/DIFF. This PIMP guardring is connected to the substrate.

[vmethod: Analysis]

Requirement DS-SELH-97 :

All guardring shall ensure a low resistive access to their respective supply VDD or GND. It is recommended to use as much as possible metal1 + contacts.

[vmethod: Analysis]

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9.2. TID HARDENING [TIDH]

9.2.1. TID mitigation at digital block level

Requirement DS-TIDH-98 :

The global margin on maximum clock frequency and setup & hold timing (cf 5.3 Digital design recommendation [DDRE]) is assumed to secure design margin regarding timing drift versus TID.

[vmethod: Simulation]

9.2.2. TID mitigation at analog block level

The primitive device list available in RD4 is the selection of the less TID sensitive devices according RD1 criterion.

Requirement DS-TIDH-99 :

It is assumed that for the TID hardening of low voltage NMOS (<= 3.3V), no special layout geometry is needed up to 100krad.

[vmethod: Analysis]

Requirement DS-TIDH-100 :

TID drift modeling is not available in the simulation model libraries. It is assumed that the unlikely worst case corner are covering the expected TID deviation on low voltage MOS. It is recommended to use an extended temperature range for critical analog performances to secure TID drift at design level.

[vmethod: Simulation]

Requirement DS-TIDH-101 :

Accordingly, the real TID drift can only be measured during TID campaign ; it is important to anticipate at design level and at TID validation test specification that fine analog performances shall be measured during the TID campaign.

[vmethod: Analysis]

Requirement DS-TIDH-102 :

It's advised to use less-sensitive primitives (e.g. resistors, capacitors, ..) when critical performance is required.

[vmethod: Analysis]

Requirement DS-TIDH-103 :

For analog MOS transistors biasing, it is recommended to be in strong inversion region ; comfortable margin shall be taken on VGS-VT and VDS –(VGS-VT).

[vmethod: Simulation]

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Requirement DS-TIDH-104 :

TID drift is sensitive to voltage biasing.

- Fully differential and linear structure are recommended.
- For power shut down mode implementation, designer shall take care to keep the symmetry in the voltage biasing (comparator inputs, current mirrors, differential pairs, etc…) to avoid differential drift under TID generating offset.

[vmethod: Analysis]

Requirement DS-TIDH-105 :

To avoid leakage current :

- N diffusion region connected to different supplies shall be separated by PDIFF ring.
- When possible, N diffusion region connected to different nets shall be separated by PDIFF ring.

[vmethod: Analysis]

9.3. SET HARDENING [SETH]

The SET mitigation in design is not independent from the top level architecture, but it is recommended to implement SET hardening at IP level to ensure an autonomous SET hardening of the PROMISE IPs.

9.3.1. SET mitigation at digital block level

Requirement DS-SETH-106 :

High drive strength buffer available in PROMISE digital library shall be used to implement the high fanout trees (clock, set and reset). Triplication + voter are also available.

[vmethod: Simulation]

Requirement DS-SETH-107 :

For non-timing critical signal where larger transition times are allowed, a built-in SET filter (around 1ns of nominal delay) is available in PROMISE library.

[vmethod: Simulation]

9.3.2. SET mitigation at analog block level

SET mitigation in analog design is mostly a trade-off between amplitude of perturbation and recovery time after. It requires systematic simulation to choose the good design solution.

IMEC make available a tool for SET simulation with a charge injection model based on literature and measurements on a similar 180nm technology. The tool uses veriloga+SKILL code, to be run on Cadence schematic. The model has limitations for a hot Nmos/Pmos (i.e. MOS transistors having bulk connected to source).

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The SET injector model uses a pre-defined set of rise and fall time constants for the double exponential charge injection current and includes voltage dependency e.g. 60 MeV.cm2/mg SET represents 1.2pC for 1.8V junctions.

Requirement DS-SETH-108 :

The IMEC SET tool shall be used to compare SET performance of different circuit implementations. It cannot be used to quantify the absolute SET hardness.

[vmethod: Analysis]

Requirement DS-SETH-109 :

Designer shall avoid the use of hot Nmos/Pmos (i.e. MOS transistors having bulk connected to source). Non compliance shall be studied case by case regarding SET.

[vmethod: Simulation]

Requirement DS-SETH-110 :

Addition of filter capacitors on static nodes e.g. biasing nodes can filter out SETs. The amount of required capacitance will be defined by simulations with the SET injection model.

[vmethod: Simulation]

Requirement DS-SETH-111 :

Too small current in biasing branches shall be avoided.

[vmethod: Simulation]

Requirement DS-SETH-112 :

High impedance nodes shall be avoided.

[vmethod: Simulation]

Requirement DS-SETH-113 :

Biasing current branches can be hardened with a feedback capacitor.

[vmethod: Simulation]

Requirement DS-SETH-114 :

Splitting transistors in multiple units/fingers is a spatial redundancy technique to limit the collected charge impact. The more general “analog averaging” redundancy technique can be applied in multiple ways on circuit and device level.

[vmethod: Analysis]

Requirement DS-SETH-115 :

Sampling systems are reducing the window of SET capturing as well.

[vmethod: Simulation]

Requirement DS-SETH-116 :

The lowest bandwidth possible to fit the performance will filter out SET pulses from previous stages.

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[vmethod: Simulation]

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Requirement DS-SETH-117 :

Capacitors for SET mitigation shall be implemented with MiM or MiM+MoM capacitor type.

[vmethod: Simulation]

Requirement DS-SETH-118 :

All critical configuration bits shall be SET filtered at the latest place in the signal path. 2 solutions :

- a built-in SET filter (around 1ns of nominal delay) is available in PROMISE library. It is used to guarantee SET integrity of non-timing critical signal where larger transition times are allowed.
- RC filter is usefull as well as the integrated SET-filter available in PROMISE library.

[vmethod: Simulation]

9.4. SEU HARDENING [SEUH]

Requirement DS-SEUH-119 :

For SEU mitigation a DICE flipflop is available in the PROMISE core cells library. The DICE flipflop includes a SET filter on the output and optionally a SET filter (1 or 2ns, depending on Low or Regular Vt version) on the DATA input.

[vmethod: Simulation]

Requirement DS-SEUH-120 :

The SEU free cells are area and power consuming ; it is recommended to trade-off use or not use hardened Flip-Flop in the data path signals.

[vmethod: Analysis]

Requirement DS-SEUH-121 :

At circuit top level, the test modes shall be gated by a primary pin of the circuit.

[vmethod: Simulation]

Requirement DS-SEUH-122 :

IMEC shall provide support for digital hardening implementation at digital front-end and back-end levels.

[vmethod: Simulation]

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10. IP DATA-PACKAGE AND SANITY CHECK [DPSC]

Requirement DS-DPSC-123 :

The full-custom mixed-signal and analog IP provider shall generate the IP data package and the necessary views to make them re-usable and compatible with the design flow as defined in AD2.

[vmethod: Analysis]

Requirement DS-DPSC-124 :

The full-custom mixed-signal and analog IP provider shall run all the checks that are defined under its responsibility in AD2.

[vmethod: Analysis]

11. COMPLIANCE MATRIX

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Référence	Description	Compliance	Verification method
DS-REQW-01	The following paragraphs are defining format and wording standard for the IP and circuits requirement specification documents :		
DS-PWRS-02	According AD3 naming convention, the power supplies name shall be : VDD1V8 / VSS1V8 VDDIO3V3 / VSSIO3V3 AVDD1V8 / AVSS1V8 AVDD3V3 / AVSS3V3 VSUB for substrate PTAP contact		
DS-PWRS-03	The Digital Core power supply VDD1V8 is 1.8V +/-10%		
DS-PWRS-04	The Digital IOs power supply VDDIO3V3 is 3V3 +/-10%		
DS-PWRS-05	The Analog power supply AVDD1V8 is 1.8V +/-10%		
DS-PWRS-06	The Analog power supply AVDD3V3 is 3.3V +/-10%		
DS-PWRS-07	The substrate connection (using PTAP) VSUB shall be handle like a power supply to ensure a low parasitic serial resistor to the GND substrate pads.		
DS-THEN-08	The block shall be functional between TJfuncmin=–40°C and TJfuncmax=125°C junction temperature and ensure cold start at TJfuncmin=–40°C junction temperature.		
DS-THEN-09	Performance requirements shall be reached between TJperfmin=0°C and TJperfmax=+105°C junction temperature. (assuming a +20°C / W RTh-JC).		
DS-RAEN-10	TID : the block shall be compatible with a 100krad minimum Total Ionizing Dose (TID).		
DS-RAEN-11	The SEU rate goal shall be less than 10-8 Ev/day/FF (or memory point) on GEO orbit while using Single Error Correction (SEC) and Double Error Detection (DEC).		

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Référence	Description	Compliance	Verification method
DS-RAEN-12	SEL immune up to a LET of 60MeV.cm²/mg.		
DS-RAEN-13	SEFI immune up to a LET of 60MeV.cm²/mg (such as unwanted reset, loss of configuration, state machine jam or transition dead state).		
DS-RAEN-14	MBU immune up to a LET of 60MeV.cm²/mg.		
DS-RAEN-15	The SET error rate to reach for the block shall be less than 10-8 Ev/day/device on GEO orbit.		
DS-RAEN-16	For high voltage MOS transistors, the Safe Operating Area shall be defined to ensure SEGR immune up to a LET of 60MeV.cm²/mg.		
DS-RAEN-17	For high voltage MOS transistors, the Safe Operating Area shall be defined to ensure SEB immune up to a LET of 60MeV.cm²/mg.		
DS-TODK-18	The latest version of documentation and design kit shall be downloaded from my.xfab.com.		
DS-DKIN-19	Design kit is configured using the XFAB xkit software. A PROMISE project shall be initialized using the following xkit initialization option : Core Module: 1 - LP (Low Power 1.8V) MOS Module: 1- MOS3 (3.3 Volt MOS) METALS: 4 - 4 Thin Metals TOPMETALS: 3 - Top and Thick Metal: METTP & METTPL FINAL_CODE = "1143"		
DS-MELA-20	The PROMISE options are supporting the following metal stack only : 6 Metal Layers: MET1 - MET2 - MET3 - MET4 – METTP – METTPL It corresponds to the module combination : MET1 - MET2 - MET3 - MET4 – METMID - METTHK		

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Référence	Description	Compliance	Verification method
DS-MELA-21	DMIM capacitor module is selected to provide the best density, linearity and matching trade-off.		
DS-PDLI-22	The exhaustive list of authorized primitive devices for IP and circuit design in PROMISE is given in RD4.		
DS-PDLI-23	The exhaustive list of primitive devices that shall not be used in IP and circuit design in PROMISE is given in RD4. They should be used only for evaluation purpose and shall not be re-used before being promoted to the authorized primitive devices list.		
DS-SPMO-24	The exhaustive list of process module for PROMISE circuit is given in RD4 according the authorized primitive list.		
DS-CORN-25	The typical junction temperature TJtyp = 25°C.		
DS-CORN-26	PROMISE digital core corners are : tm / VDD1V8typ/ TJtyp + (ws/wp X VDD1V8min/max X TJfuncmin/TJfuncmax) Giving 1 + (2x2x2) = 9 corners for digital core cells simulations.		
DS-CORN-27	PROMISE digital IOs corners are : tm / VDD1V8typ / VDDIO3V3typ / TJtyp + (ws/wp X VDD3V3min/max X VDD1V8min/max X TJfuncmin/TJfuncmax) 1.8V and 3.3V are correlated. Giving 1 + (2x2x1x2) = 9 corners digital IOs simulations.		

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Référence	Description	Compliance	Verification method
DS-CORN-28	PROMISE analog functional corners are : tm / AVDD1V8typ / AVDD3V3typ / TJtyp + (ws/wp X AVDD1V8min/max X AVDD3V3min/max X VDD1V8min/max X VDDIO3V3min/max X TJfuncmin/TJfuncmax) 1.8V and 3.3V are correlated. Analog and digital supplies are correlated. Giving 1 + (2x2x1x1x1x2) = 9 corners for analog functional simulations.		
DS-CORN-29	PROMISE analog performance corners are : tm / AVDD1V8typ / AVDD3V3typ / TJtyp + (tm/ws/wp/wo/wz X AVDD1V8min/max X AVDD3V3min/max X VDD1V8min/max X VDDIO3V3min/max X TJperfmin/TJperfmax) Giving 1 + (5x2x1x1x1x2) = 21 corners for analog performance simulations, if all power supplies are correlated.		
DS-CORN-30	Analog performance corners shall be adapted to the simulated circuit by including all other contributor as resistors, capacitors, etc…		
DS-CORN-31	Eventual non correlation between analog 1.8V and 3.3V and between analog and digital supplies shall be taken into account to define the corners.		
DS-CORN-32	Analog performance drift range could be defined inside the performance range.		

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Référence	Description	Compliance	Verification method
DS-CORN-33	Digital Top-Level Sign-off corners are : tm / VDD1V8typ / VDDIO3V3typ / AVDD1V8typ / AVDD3V3typ / Ttyp + (ws/wp X AVDD1V8min/max X AVDD3V3min/max X VDD1V8min/max X VDDIO3V3min/max X Tfuncmin/Tfuncmax) 1.8V and 3.3V are correlated. Analog and digital are correlated. Giving 1 + (2x2x1x1x1x2) = 9 corners		
DS-CORN-34	Monte-Carlo simulations shall be performed using at least 3 sigma dispersion for wafer lot dispersion and devices mismatch.		
DS-CORN-35	For critical analog performances related to devices mismatch (offsets, bandgap voltages, etc…), it is recommended to run Monte-Carlo simulation using devices mismatch in combination with worst case corners.		
DS-PADR-36	Designer shall use the analog and digital pads available in the IOs libraries available for PROMISE. (cf RD3).		
DS-PADR-37	For ESD performances and protection strategy, refer to RD3 and the ESD documentation on "my X-FAB".		
DS-PADR-38	IMEC may provide some advises and basic tools to support padring design.		
DS-PADR-39	The padring shall be defined using a .csv table including the following columns : The file may be used as a unique database to generate cell views (schematic, layout).		
DS-DDRE-40	A 25ps margins shall be taken into account on hold timing to cover uncertainty on contributors.		

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Référence	Description	Compliance	Verification method
DS-DDRE-41	Globally, a 10% margin shall be applied on the maximum clock frequency to cover setup margin, TID drift and an ageing margin that are not taken into account in .lib timings.		
DS-DDRE-42	IMEC shall provide support to implement the digital power grid and common rules for digital placement and routing.		
DS-ADRE-43	Never connect a low voltage (1V8) gates directly to a supply (power or ground). Dedicated tie cells must be used to prevent ESD stress on the thin gate of the transistor (cf RD7).		
DS-ADRE-44	Never connect IO transistor gates directly to a supply (power or ground). Dedicated tie cells must be used to prevent ESD stress on the thin gate of the transistor (cf RD7).		
DS-ADRE-45	If a clock is used between an analog IP and the digital core, it is recommended that the analog IP provides the clock for data synchronization to the digital core (even if the clock is initially provided by the digital core)		
DS-ADRE-46	The required views for an analog block in a digital flow are defined in AD2. Basically, a .lib file including all arcs in all modes and a simple .v (connectivity) are required. For mixed-signal simulations of analog blocks, a .va (behavioral Verilog A model) is very useful. Such behavioral model can go from very simple to very complex. The designer should define clearly the limitations of the .va behavioral model in the IP datasheet. The main modes of the IP should be modeled. Correlation of the .va model with spice models is needed. Only the typical corner is enough for the .va model and the comparison.		
DS-ADRE-47	Each analog IP shall be provided with a power down command.		

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Référence	Description	Compliance	Verification method
DS-ADRE-48	The power-up and power-down sequences shall be simulated while verifying the Safe Operating Area.		
DS-LREC-49	A dedicated PIN named VSUB shall be used for substrate PTAP contact ; this VSUB pin is common to all IPs and is connected at top level to a dedicated PIN of the chip.		
DS-LREC-50	All IPs shall have : a DNWELL or DNWELLMV ring at the periphery. a n+ ring + metal1 to contact the DNWELL or DNWELLMV to the related VDD supply. a wide substrate PTAP + metal1 ring around the IP, outside the DNWELL or DNWELLMV ring. This ring is connected via the PIN VSUB.		
DS-LREC-51	The IP pins shall be defined at the IP periphery and its geometry shall correspond to the metal width to be connected.		
DS-LREC-52	The layout shall implement as much as possible contacts and vias. A minimum of 2 vias or contacts shall be implemented in analog IPs.		
DS-LREC-53	For internal analog IPs only, and when there is no impact on performances, a derating factor of 50% shall be taken regarding the current density parameters vs electro migration (wires, vias, contact). For digital design, electro migration shall be consistent with XFAB rules without specific margin.		
DS-LREC-54	To avoid missing connection at upper level, the connect-by-name option in LVS is forbidden at all level of hierarchy. Accordingly, interfaces of all supplies and interfaces shall be made using a unique pin.		
DS-INCO-55	Digital block shall be supplied by the unique digital core supply VDD1V8. Different digital core power domain are forbidden.		

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Référence	Description	Compliance	Verification method
DS-INCO-56	Cross power domains (VDD1V8 from-to AVDD1V8, from-to VDDIO3V3, from-to AVDD3V3) shall be handled by the relevant level shifters inside the analog block. PROMISE library provides cross domain level shifter with pull-up or pull-down behavior during power-on when the CORE VDD1V8 supply is not present (Power On Reset block output can be used). The level shifters include the proper ESD strategy at power domain change.		
DS-INCO-57	To avoid glitches at digital outputs during power-on, the digital IO buffer with Power-On-Control system shall be used (Cf RD3).		
DS-TEST-58	The goal of digital Design For Test are : Scan stuck-at : coverage > 98% Memory BIST (at speed) Boundary scan		
DS-TEST-59	The scan version of the hardened FF shall be SEU used.		
DS-TEST-60	If registers are used to configure test mode, the related FF shall be SEU hardened and gated by primary pin of the circuit.		
DS-TEST-61	For hard macros (i.e. all blocks having a layout view), the digital DFT shall be embedded with the IP. The required views and files are defined in AD2. Note : All blocks designed in the frame of PROMISE project are hard macros.		
DS-TEST-62	For soft macros (i.e. IPs at RTL level), DFT can be handled at top level if : All Clocks are controlable through dedicated bypass All asynchronous Reset are controllable through dedicated bypass All synchronous reset areindependent from asynchronous reset in scan mode		
DS-TEST-63	All memories must be bypassed in scan mode.		

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Référence	Description	Compliance	Verification method
DS-TEST-64	All bidirectional IOs shall be in a defined state during test mode.		
DS-TEST-65	Precaution must be taken for Memory BIST insertion : the number of MBIST controller shall be traded-off versus area and at speed capability.		
DS-TEST-66	The proposed strategy is to handle the analog multiplexing of all analog test signal at top level through a low bandwidth test connection dedicated to the 2 analog power domain (AVDD3V3 and AVDD1V8).		
DS-TEST-67	The analog test switches shall be of T type : 2 serial MOS switches and in the middle a parallel MOS switch to the GND (to limit noise coupling across the test network). If the leakage current in the MOS to GND has impact on analog performances, this MOS may be connected to a voltage between GND and VDD. The 2 serial switches shall have different digital command signal to contribute to SET mitigation.		
DS-TEST-68	The switches control logic driver shall use SET free circuitry (cf SET hardening chapter).		
DS-TEST-69	The top level digital core shall handle the control and decoding of all analog test switches. The decoder shall avoid any simultaneous command of different test switches.		
DS-TEST-70	All the analog test signal shall be connected in a daisy chain mode at top level to 2 differential pads per analog power domain : ana-testout_p_1V8 and ana-testout_n_1V8 ana-testout_p_3V3 and ana-testout_n_3V3		
DS-TEST-71	The tested signal shall not be disturbed by the analog test circuitry and remain in a known and representative state (no induced oscillation, etc…).		

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Référence	Description	Compliance	Verification method
DS-TEST-72	If high bandwidth testability needs to be implemented, it shall be fully handled and implemented at IP design level independently to the standard low bandwidth testability.		
DS-PWRO-73	A PROMISE circuit shall embed the Power On Reset block (cf RD6). An internal LDO may be used to generate the internal 1.8V from the external 3.3V supply.		

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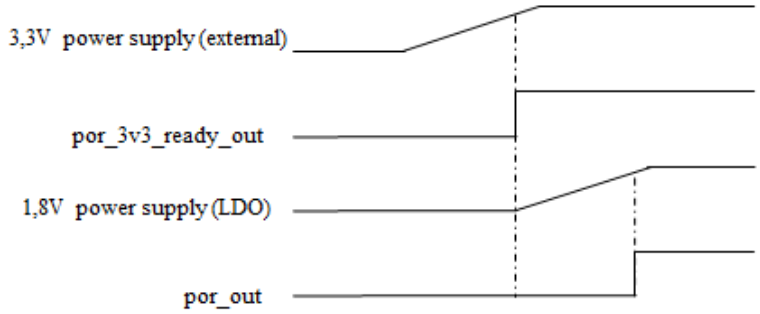
Référence	Description	Compliance	Verification method
DS-PWRO-74	Based on this architecture at circuit top level, the Power-ON sequence shall be : Power-on of the external 3.3V power supply At power-on, the POR sets its reset output signals at “0”. When the 3.3V power supply voltage reaches the POR threshold, the POR rises 3V3_ready signal at “1”. POR reset output signals stays at “0”. 3V3_ready signal is used as an enable to start the PROMISE BG and LDO 1V8 IPs : The bandgap starts with initial trimming The LDO1V8 generates the 1.8V supply from the 3v3 external power supply When the 1.8V supply voltage reaches the POR threshold, the POR set its reset output signal at “1”. This reset signal is used by others IPs in PROMISE ASSP to release their reset state. The circuit is operated nominally and the BG can be trimmed using digital interface or trimming code stored in the NVM.  Figure 2 : Power-ON sequence		

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Référence	Description	Compliance	Verification method
DS-NACO-75	The pins type and direction (input, output, etc…) shall be defined and consistent across the design hierarchy.		
DS-NACO-76	The naming conventions shall fulfill the requirements as described in AD3		
DS-DFLO-77	The PROMISE circuit design flows options are described in AD2. The baseline design flow for a digital, an analog or mixed circuit is Digital-on-top (i.e. digital P&R does the circuit top-level ; the design flow handles the design from RTL to GDSII). Analog-on-top methodology can be used for pure analog circuit.		
DS-DFLO-78	Mixed-signal or analog IPs useful views and data package to be integrated in the PROMISE library are described in AD2. Some specific views to be handled by the digital P&R tool in a digital-on-top design flow require an additional design effort versus a usual analog full-custom design flow, but digital-on-top design flow ensures the highest level of intellectual property protection and the highest level of reusability.		
DS-DFLO-79	All analog/mixed-signal IP must be simulated using the analog functional corners to extract the timing models. (Those corners are consistent with the digital corners to allow consistent digital-on-top design flow).		
DS-TOSE-80	Due to limited knowledge of such tools at IMEC and to avoid any problem in case difference in IP simulation results, verification results, etc…, the tools set for final data package in PROMISE library is restricted to the tools defined in AD2.		

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Référence	Description	Compliance	Verification method
DS-TOSE-81	Upon design house responsibility, a different design tool set can be used during the IP detailed design phase, but the IP data package shall be fully verified by the design house using the PROMISE tool set to be promoted to the PROMISE library.		
DS-DKVU-82	It is highly advised to the IP design house to verify the impact of the new design kit version on its existing PROMISE IPs. At IP design level, a proper design and verification data organization may help to run with low effort a non-regression verification with a new XFAB design kit version.		
DS-DMET-83	Verify the good understanding of IP or Circuit requirement specification during the Kick-Off and Input Specification review. Identify all requirement that may be changed by the customer and the requirements that can be traded-off.		
DS-DMET-84	During the definition phase, in addition to the AD1 guidelines, clearly define the main architecture aspects that will drive the architecture analysis. These main architecture aspects shall be presented to the customer and agreed with him during the System requirement review.		
DS-DMET-85	During the architectural design, in addition to the AD1 guidelines, the top level symbol shall be finalized, as well as the first floor plan defining the position of the interfaces. The behavioral model shall be created to start verifying the main functional requirements. It is important to also take into account all the testability and validation constraints at architecture level. The sub blocks detailed specification shall be also defined and included to the verification plan and compliance matrix in relation with the top level requirements.		

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Référence	Description	Compliance	Verification method
DS-DMET-86	During the detailed design phase, in addition to the AD1 guidelines, the simulation plan shall be fully defined and implemented in the CAD tools in parallel of the schematic creation. The coverage of the requirements shall be exhaustively verified using the compliance matrix template provided in the circuit specification. Only start the detailed devices sizing when simulation plan is fully implemented.		
DS-DMET-87	The detailed layout shall be only started after the Detailed design review. To avoid any re-design / re--layout loops.		
DS-DMET-88	The methodology shall be implemented at each level of the design ; for lower level blocks, the formalism can be reduced, but the philosophy shall be respected.		
DS-DMET-89	For the top level design (IPs or ASIC), the methodology shall be 100% respected.		
DS-DERE-90	A Kick-Off and Input Specification review shall be schedule at the very beginning of the design activities to assess the good understanding of all the items of the IP requirement specification.		
DS-DERE-91	During the IPs and top level circuit design activities, the reviews defined in AD1 shall be held.		
DS-DOC-92	The design documentation shall follow the recommendation in AD1. The content and the format will be designer-friendly oriented while fulfilling a high level of compliance with AD1.		
DS-DOC-93	The Design documentation issued during the design phase of PROMISE IPs and Pilot Circuit may be used as template for future design activities (after removing non disclosable information).		

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Référence	Description	Compliance	Verification method
DS-SELH-94	The main mitigation for SEL in bulk CMOS technology is the use of systematic diffusion guardrings to separate NMOS from PMOS : NIMP/DIFF guardring at the periphery of NWELL PIMP/DIFF guardring at the periphery of PWELL		
DS-SELH-95	Mixed signal-design are taking advantages in the use of triple-well (ISOMOS module). Each DNWELL area shall be implemented with : NWELL+NIMP/DIFF guardring at the periphery of the DNWELL PIMP/DIFF guardring around the DNWELL. This PIMP guardring is connected to the substrate.		
DS-SELH-96	If ISOMOS module is not used, PIMP/DIFF guardring shall be implemented around the NWELL and NIMP/DIFF. This PIMP guardring is connected to the substrate.		
DS-SELH-97	All guardring shall ensure a low resistive access to their respective supply VDD or GND. It is recommended to use as much as possible metal1 + contacts.		
DS-TIDH-98	The global margin on maximum clock frequency and setup & hold timing (cf 5.3 Digital design recommendation [DDRE]) is assumed to secure design margin regarding timing drift versus TID.		
DS-TIDH-99	It is assumed that for the TID hardening of low voltage NMOS (<= 3.3V), no special layout geometry is needed up to 100krad.		
DS-TIDH-100	TID drift modeling is not available in the simulation model libraries. It is assumed that the unlikely worst case corner are covering the expected TID deviation on low voltage MOS. It is recommended to use an extended temperature range for critical analog performances to secure TID drift at design level.		

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Référence	Description	Compliance	Verification method
DS-TIDH-101	Accordingly, the real TID drift can only be measured during TID campaign ; it is important to anticipate at design level and at TID validation test specification that fine analog performances shall be measured during the TID campaign.		
DS-TIDH-102	It's advised to use less-sensitive primitives (e.g. resistors, capacitors, ..) when critical performance is required.		
DS-TIDH-103	For analog MOS transistors biasing, it is recommended to be in strong inversion region ; comfortable margin shall be taken on VGS-VT and VDS –(VGS-VT).		
DS-TIDH-104	TID drift is sensitive to voltage biasing. Fully differential and linear structure are recommended. For power shut down mode implementation, designer shall take care to keep the symmetry in the voltage biasing (comparator inputs, current mirrors, differential pairs, etc…) to avoid differential drift under TID generating offset.		
DS-TIDH-105	To avoid leakage current : N diffusion region connected to different supplies shall be separated by PDIFF ring. When possible, N diffusion region connected to different nets shall be separated by PDIFF ring.		
DS-SETH-106	High drive strength buffer available in PROMISE digital library shall be used to implement the high fanout trees (clock, set and reset). Triplication + voter are also available.		
DS-SETH-107	For non-timing critical signal where larger transition times are allowed, a built-in SET filter (around 1ns of nominal delay) is available in PROMISE library.		
DS-SETH-108	The IMEC SET tool shall be used to compare SET performance of different circuit implementations. It cannot be used to quantify the absolute SET hardness.		

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Référence	Description	Compliance	Verification method
DS-SETH-109	Designer shall avoid the use of hot Nmos/Pmos (i.e. MOS transistors having bulk connected to source). Non compliance shall be studied case by case regarding SET.		
DS-SETH-110	Addition of filter capacitors on static nodes e.g. biasing nodes can filter out SETs. The amount of required capacitance will be defined by simulations with the SET injection model.		
DS-SETH-111	Too small current in biasing branches shall be avoided.		
DS-SETH-112	High impedance nodes shall be avoided.		
DS-SETH-113	Biasing current branches can be hardened with a feedback capacitor.		
DS-SETH-114	Splitting transistors in multiple units/fingers is a spatial redundancy technique to limit the collected charge impact. The more general “analog averaging” redundancy technique can be applied in multiple ways on circuit and device level.		
DS-SETH-115	Sampling systems are reducing the window of SET capturing as well.		
DS-SETH-116	The lowest bandwidth possible to fit the performance will filter out SET pulses from previous stages.		
DS-SETH-117	Capacitors for SET mitigation shall be implemented with MiM or MiM+MoM capacitor type.		
DS-SETH-118	All critical configuration bits shall be SET filtered at the latest place in the signal path. 2 solutions : a built-in SET filter (around 1ns of nominal delay) is available in PROMISE library. It is used to guarantee SET integrity of non-timing critical signal where larger transition times are allowed. RC filter is usefull as well as the integrated SET-filter available in PROMISE library.		

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Référence	Description	Compliance	Verification method
DS-SEUH-119	For SEU mitigation a DICE flipflop is available in the PROMISE core cells library. The DICE flipflop includes a SET filter on the output and optionally a SET filter (1 or 2ns, depending on Low or Regular Vt version) on the DATA input.		
DS-SEUH-120	The SEU free cells are area and power consuming ; it is recommended to trade-off use or not use hardened Flip-Flop in the data path signals.		
DS-SEUH-121	At circuit top level, the test modes shall be gated by a primary pin of the circuit.		
DS-SEUH-122	IMEC shall provide support for digital hardening implementation at digital front-end and back-end levels.		
DS-DPSC-123	The full-custom mixed-signal and analog IP provider shall generate the IP data package and the necessary views to make them re-usable and compatible with the design flow as defined in AD2.		
DS-DPSC-124	The full-custom mixed-signal and analog IP provider shall run all the checks that are defined under its responsibility in AD2.		

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APPENDIX A : ANNEX 1

Internal code / DRL	Location of record
AD1	http://ecss.nl/get_attachment.php?file=standards/ecss-q/ECSS-Q-ST-60-02C31July2008.pdf http://ecss.nl/get_attachment.php?file=standards/ecss-q/ECSS-Q-ST-60-02C31July2008.doc
AD2	PROMISE document repository
AD3	PROMISE document repository

Internal code / DRL	Location of record
RD1	http://ecss.nl/get_attachment.php?file=2016/09/ECSS-Q-HB-60-02A1September2016.pdf
RD2	https://my.xfab.com
RD3	PROMISE document repository
RD4	PROMISE document repository
RD5	https://www.xfab.com/service/design-support/eda-partners/
RD6	PROMISE document repository
RD7	PROMISE document repository

END OF DOCUMENT

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